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Integrated Optoelectronic Receivers

S. R. Forrest
SDSU Foundation

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Described here is the first phase of a 3-year program for the fabrication of highly sensitive, monolithically integrated optical receivers for fiber optic communication systems operating in the 1.3- to 1.55-μm range. The significant progress in this work has been the growth, by liquid phase epitaxy, of high purity, high uniformity InP and $In_{0.53}Ga_{0.47}As$ layers suitable for photodiode and FET applications, fabrication of a very low dark current, low capacitance $In_{0.53}Ga_{0.47}As$ p-i-n photodiode, identification, and complete analysis of $In_{0.53}Ga_{0.47}As$ and InP self-aligned JFET structures. The result is that $In_{0.53}Ga_{0.47}As$ is identified as the material which is preferable for use in integrated receivers, and the fabrication of a discrete $In_{0.53}Ga_{0.47}As$ JFET. The progress of this research effort should be continued over the next 2 years such that the initial goals of a fully integrated, high sensitivity receiver can be realized.

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I. Introduction

Considerable effort has recently been expended in developing integrated optical sources and detectors for systems with increased bandwidth and functionality. The driving force of this effort has been the reduced cost and increased reliability of integrated circuits compared to their hybrid counterparts. Unfortunately, the integrated circuits that have been made at various laboratories in the United States, Europe and Japan have not met the theoretical performance expected of them. There are at present no published examples of monolithically integrated optoelectronic circuits which match the performance of similar optimized hybrid circuits. It has been recognized particularly for applications such as communications, local area networks and optical signal processing that integrated optoelectronic components[1] such as lasers and LED array transmitters, modulators, and photodiode receiver arrays[2] will play a central role. The challenge here is to develop inexpensive integrated devices requiring minimum power consumption and exhibiting little optical or electrical interactions between neighboring devices. In addition to the above applications, it is important to recognize the applications of such receivers to coherent transmission systems whereby photoreceivers consisting of a 1x2 photodiode array and a differential amplifier are required for PSK systems. Such a monolithic device is a natural and simple extension of the proposed work. Furthermore, detector arrays can be used for wavelength division multiplexed schemes whereby the multiwavelength beam is incident on a grating which then spatially separates the various beams onto the array elements.

The successful development of these technologies requires high quality photonic and electronic components, as well as a means of integrating and interfacing these two circuit segments which often have conflicting materials requirements.

It should be noted that there is considerable motivation to work on InP-based materials in addition to GaAs-based systems for use in optoelectronic integrated circuits. This motivation stems primarily from:

1) The higher electron mobilities, effective drift velocities and/or peak velocities of InP-based alloys--particularly InP and $In_{0.53}Ga_{0.47}As$--imply that higher speed operation can be achieved in devices using these materials in place of GaAs-based transistors.

2) The ternary compound $In_{0.53}Ga_{0.47}As$ has a bandgap of 0.75 eV, and therefore can detect light at both the short wavelengths available to the GaAs-based devices (0.8-0.9 μm) as well as the long wavelengths used in optical communication systems (1.3 μm and 1.55 μm). Such a wavelength versatility is unavailble to the GaAs-based alloys.

3) This is a more highly "leveraged" material system. That is, the desirability to use a common material system for devices employed on-premises (in applications such as local area networks, optical interconnects, and optical signal processing) as well as off-premises (such as long-haul transmission) increases as the level of system interconnectivity increases. As distances between terminals increase, long-wavelength, InP-based transmitters and receivers must be employed. Thus, to increase the level of component integration, and to reduce the number of interfaces where prior thought must be given

as to the type of componentry needed, it is apparent that InP-based devices have a more universal application.

4) InP has the largest bandgap (1.35 eV) of any of the alloys of InGaAsP which can be epitaxially grown on these substrates. This situation, which is opposite to that which adheres in the GaAs-based materials system, implies that InP forms a substrate which is transparent to the incident radiation (provided that the long wavelength "window" is used). Such transparent substrates provide a distinct advantage in optical receivers where the optical coupling can be made extremely efficient when the light is incident on the detector via the substrate. Also, these transparent substrates are particularly advantageous for use in optical computing systems, where two-dimensional spatial light modulator arrays require the light to be incident, or otherwise leave, via the device substrate.

5) As in the case of AlGaAs/GaAs, $In_{0.53}Ga_{0.47}As$ lattice-matched to semi-insulating $In_{0.52}Al_{0.48}As$ or InP can be useful in high performance MODFET structures.

One final reason which makes it desirable to investigate InP-based materials is that there is a general lack of emphasis on integrating this alloy system in laboratories worldwide. Indeed, the preponderance of work on monolithic optoelectronic integration is focused on the GaAs system for use in local area network systems. This work, being carried out ostensibly in Japan, presently ignores many of the other important systems applications being addressed in this work. On the other hand, the state-of-the-art in discrete photonic devices is well advanced in the InP-based systems, giving a strong starting point from which to pursue integration problems.

Although high quality photonic components have been demonstrated, notably absent from devices based on InP and related compounds is the demonstration of a good transistor technology.[1] As discussed above, properly designed transistors made from InGaAs promise to have higher performance than GaAs, and should result in improved electronic circuits as well as optoelectronic components which take advantage of the greater transparency and lower dispersion of silica fibers at long-wavelengths as opposed to the short-wavelength (0.8-0.9 μm) window available to GaAs-based circuits. In the future, we expect that the highest speeds will be attained using both electronic and photonic interconnects integrated directly into large scale circuits. For such a goal to be realized, InGaAs may provide extremely high speed switching at room-temperature, and therefore is an important material to study with these applications in mind.

The research goals of this collaboration between USC and the Naval Ocean Systems Center in San Diego are to address several of these issues with the aim of improving integrated devices made from InP-based alloys, and to obtain a deeper understanding of the limits of the technologies involved in the growth of these materials. The work concentrates on developing a framework and technology for high-performance optoelectronic device fabrication and design using these critically important materials.

There are a variety of issues which must be faced in order to actually produce a high quality integrated optoelectronic circuit. Some of these are well defined and some are rather elusive. The major technical issues are:

1. The need for high quality epitaxial material which can be grown with controllable doping concentrations and thicknesses and which are defect free. In addition, an advanced growth technique of selective growth of one material within another will have to be developed in order to meet the conflicting requirements of the detector (high resistivity for a wide, depleted absorption region, and long wavelength sensitivity via a small bandgap) and the transistor material (high conductivity for high gain).
2. The development of a reliable planar technology for selectively grown III-V compound materials. This requirement arises from the need for reliability and for low total capacitance at the input of the first transistor. A planar surface to operate on with photolithographic masks also increases line definition (and therefore bit rate) and relieves the requirement for etching mesas with gradually sloping sides to accommodate metal interconnects from one device to the next.
3. Independent optimization of materials used for the optical and electronic parts of the circuit. Contradictory requirements are particularly conspicuous in a receiver, wher the detector requires a low doped, thick optical absorbing region, and the transistors usually require thin, highly doped channel layers. These devices must then be interconnected with a very low parasitic capacitance metal pattern.
4. The question of the minimum electronic circuit required to successfully demonstrate the theoretical sensitivity at the chosen bit rate. Previous efforts at integration have employed one or two transistors and a few resistors in addition to the photodiode itself. When tested, a low capacitance probe or an FET is bonded in hybrid fashion to the chip. The question is: "Does the interface with the

surement probe degrade the chip performance?" More importantly, it must be decided just how much of the circuit must be included on the chip and how much can afford to reside off the chip.

5. A high transconductance (and hence gain) is required for the first FET. A proper transistor technology must be chosen which will provide as high a transconductance as possible. Just as important as transconductance is a reliable FET technology which can supply the proper gains, currents, and impedances demanded by the circuit design. For InP based materials, the technology as a whole is far less developed than the GaAs MESFET technology. (Also, see Appendix A.) On the other hand, JFETs have recently been found to show promise in the InP-based materials system,[4,5] although they are somewhat complex to fabricate. The appropriate choice of transistor structures and materials requires a sophisticated assessment of the advantages and drawbacks of each different type of FET and a mature, balanced approach calculated to obtain the maximum performance out of the ultimate circuit.

As will be discussed in the following sections, we have made significant progress in the first year of this three year program toward answering these numerous and fundamental questions concerning InP-based optoelectronic integrated circuits (OEICs). It is expected that by the completion of this program, a high performance OEIC receiver fabricated in this materials system will be realized.

II. Materials Growth

Using our high purity, high uniformity LPE system, we have concentrated on growing InGaAs and InGaAs/InP heterojunctions for FET and p-i-n detector applications. The LPE system consists of two furnaces (now being expanded to 4), whereby one is used for source bakeout, and the other for layer growth. Growth is accomplished by the two-phase technique. Furthermore, uniformity of the layers is due to our somewhat unconventional boat design. During growth, the wafer is maintained at a single location in the center of the three zone, 24 inch furnace, while the boat *body* is translated. In this manner, the growth always occurs at the same furnace location, thereby maintaining controlled thermal conditions. Surface preservation during the initial, warm-up and homogenization cycle is achieved by preparing all sources and wafers in the same clean room as the growth system. The loading area of the LPE furnaces is kept under an additional laminar flow environment whose cleanliness may be as high as class 100.

Typically, the doping of the InGaAs and InP layers are 2×10^{15} cm^{-3} and 5×10^{15} cm^{-3}, respectively. A typical free carrier concentration profile for the InGaAs and InP layers is shown in Fig. 1. The free carrier concentration in these layers is observed to be very uniform throughout the layer thickness, and the material interfaces appear sharp and uniform as well. Here, we have profiled the wafers using the non-destructive organic-on-inorganic (OI) semiconductor wafer analysis technique introduced by the Forrest, and co-workers[6] in 1985. This means of analysis uses capacitance-voltage (C-V) data obtained by reverse-biasing the OI contact such that the inorganic epitaxial material is depleted to distances far from the wafer surface. The OI technique is routinely used in our laboratory as quality

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OPERATOR: Rec. TIME: 16:26:33

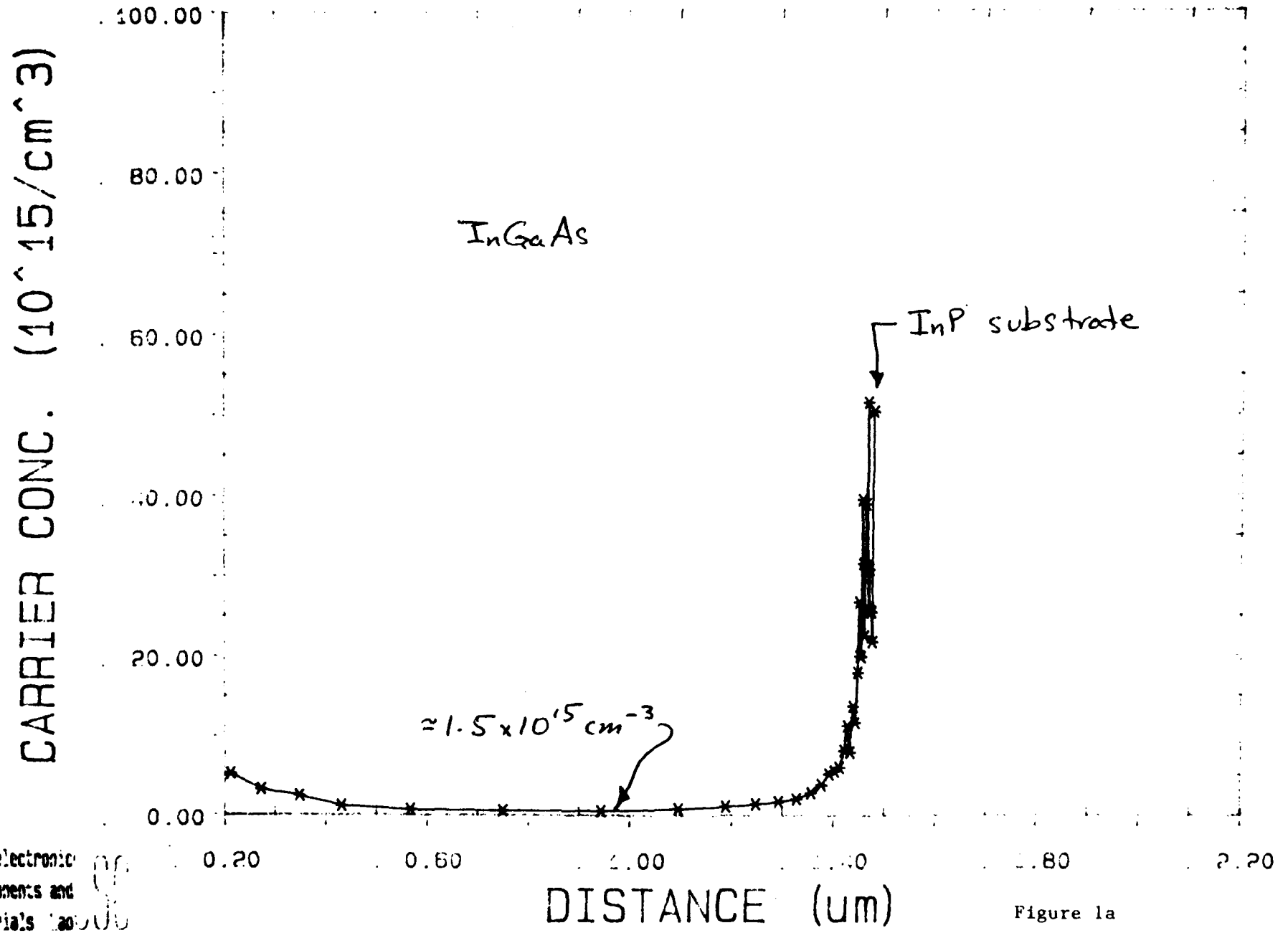

Figure 1a

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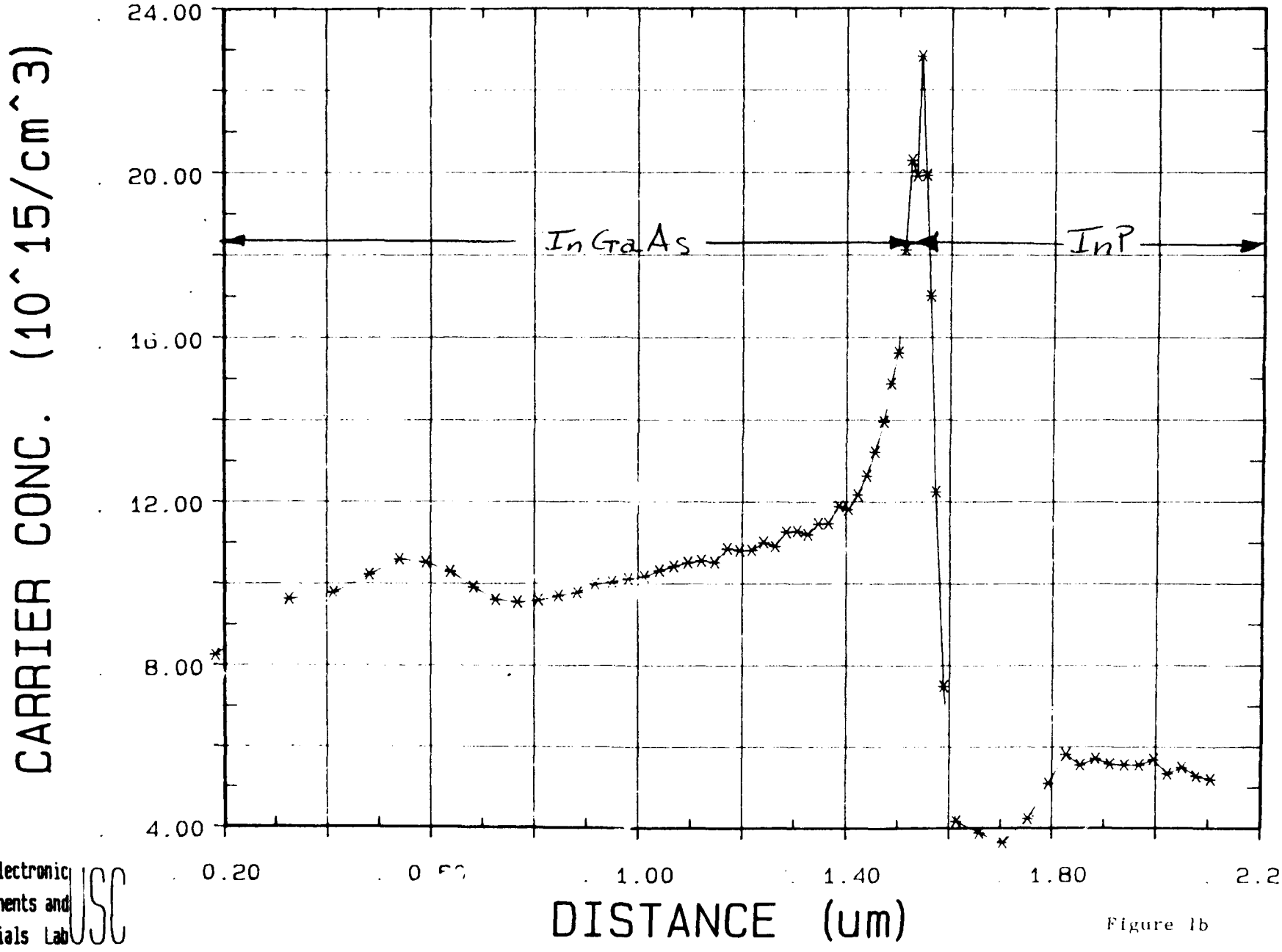

Optoelectronic Components and Materials Lab USC

Figure 1b

control measure for assessing wafer growth. Note in Fig. 1b the peak and valley in the profile which exists at the InGaAs/InP heterointerface. This feature is located within 100 - 200 A of the actual heterojunction, and therefore serves as a means of measuring the HJ depth from the wafer surface. The sharpness of the feature is also an indication of the abruptness of the HJ (approximately 100 - 300 A for our material).

The lattice mismatch between the InGaAs and InP layers is typically less than 0.02% as measured using our Rigaku double crystal diffractometer. A typical rocking curve for one such HJ structure is shown in Fig. 2. Excellent lattice match is indicated by the inability to resolve diffraction peaks due to the InP and $In_{0.53}Ga_{0.47}As$ layers. From the width of the peak, a lattice mismatch of -0.016% is inferred. The surface morphology of the as-grown layers is highly uniform, with only a very slight ripple appearing across the entire 16 x 16 mm wafer. Once again, we attribute the excellent surface morphology to the means by which the wafer is maintained at a fixed location in the furnace while the boat body is translated. Growths have been accomplished on both n^+ and semi-insulating substrates.

To satisfy the needs for monolithic integration of a detector and an adjacent transistor circuit, we have pointed out in Sec. I the need to separately optimize the detector and the FET material. This is done by growing the ternary material in a pre-etched well in a semi-insulating substrate, followed by the growth of the FET material. To initiate this study, we have succeeded in growing InGaAs in pre-etched wells in the semi-insulating substrate. In this work, wells 5 μm deep were chemically etched in the semi-insulating substrate. Growth of InGaAs over the full wafer surface to a thickness of 5 μm deep in 100 x 150 μm well was accomplished.

SAMPLE NAME:B-08098
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VOL and CUR: 40KV 30mA
SLITS :1st 1 2nd .05 3rd 1
SCAN SPEED: 50 SEC/MIN.
STEP/SAMPL.: 1 SEC
PRESET TIME: 0 SEC
FILE NAME :8098100
OPERATOR :CDL
COMMENT :

DATE:88.08.09

No.	Omega	INTEN.	gW	Io/Is	dD/D
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2	24	5094	20	46	-1.5718E-04

Sample Name : B-08098

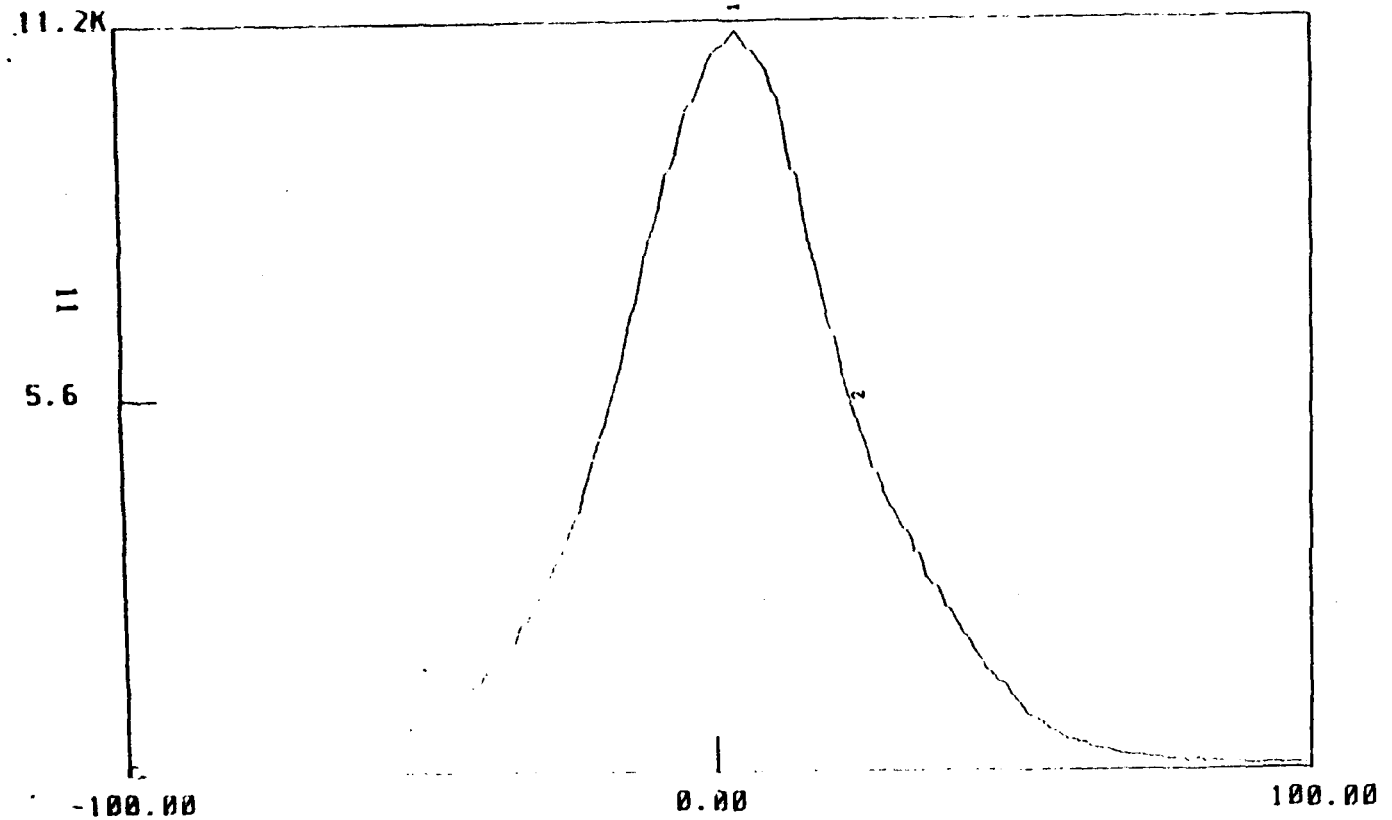


Figure 2

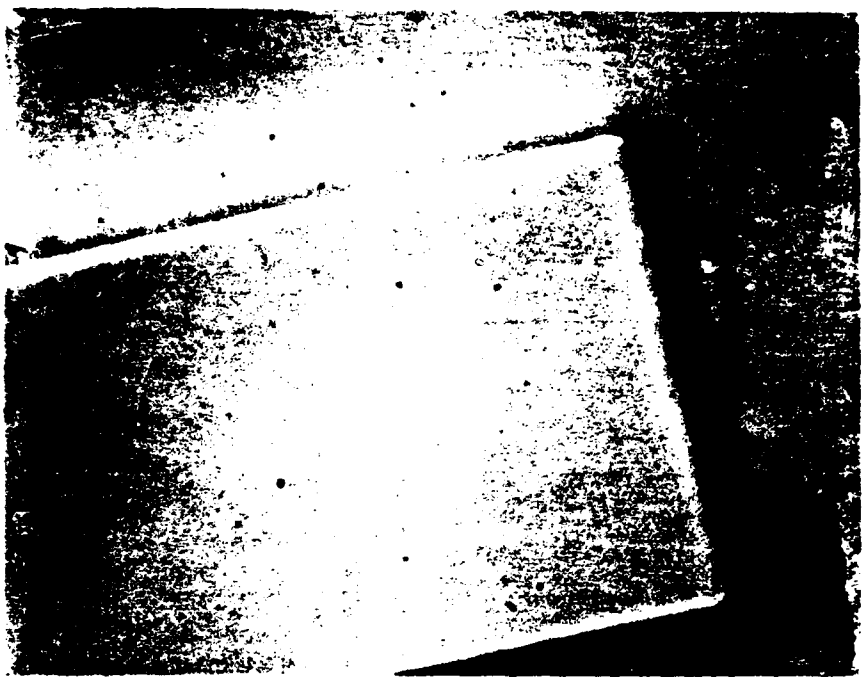
We note that growth in the well is somewhat faster than on the free InP surface. Furthermore, to maintain well geometry, the growth was done without substrate melt-back, and without the growth of an InP buffer layer. Successful elimination of both of these steps is an indication of wafer cleanliness, and the efficacy of the In-Sn basket in achieving good surface preservation.

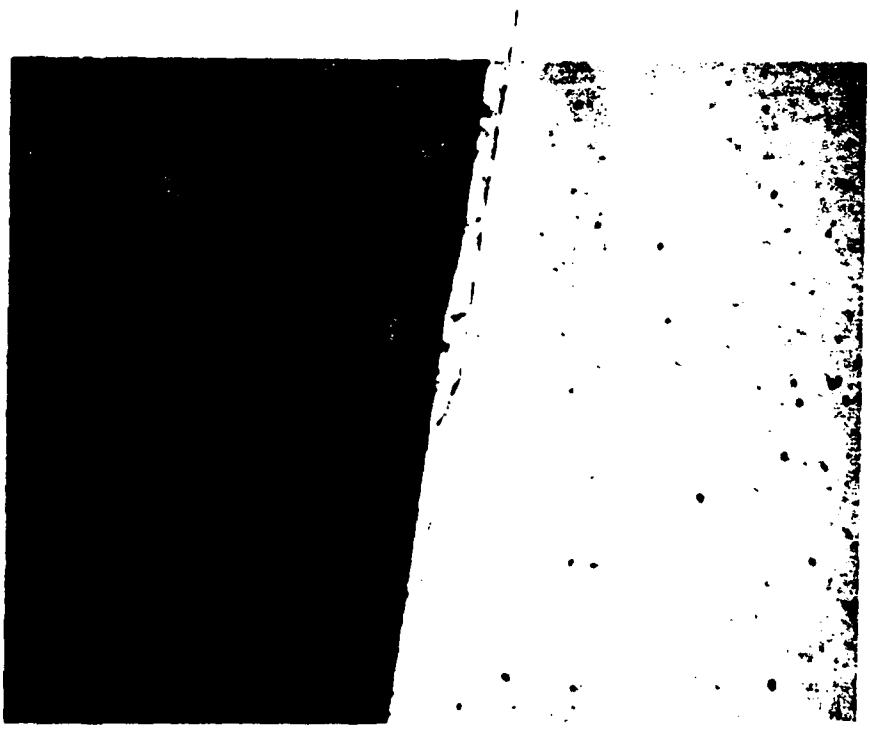
After growth, the wafer is re-masked, and the InGaAs grown outside the well is removed using a materials selective etchant (H_2SO_4:H_2O_2:H_2O in a ratio of 5:1:1). Microscopic views of the material grown in wells is shown in Fig. 3. Here, we see reasonably good filling of the well with only a slightly uneven surface near the well edge. It is expected that considerably superior results will be obtained as we become more experienced at the well-growth process.

III. Detector results

To provide for monolithic integration of the detector and JFET circuit, we have generated a mask set to fabricate 40 μm diameter planar, InGaAs p-i-n detectors in wells pre-grown in an InP substrate. Planar p-i-n detectors were first attempted in this work using the structure shown in Fig. 4. Starting with S-doped, (100) InP substrates, an approximately 1-2 μm thick, undoped InP buffer layer is grown, followed by a 5 μm thick InGaAs light absorbing region. Next, a 1000 A thick SiN_x layer was deposited. A 40 μm diameter hole was chemically etched in the insulating layer through which Zn was diffused to form the p-n junction.

Prior to junction formation, it was necessary to establish the conditions for diffusion for both the p-i-n detector (with a diffusion depth, x_j, of approximately 2 μm) and the JFET (where x_j = 0.5 μm) to be





InGaAs / InP

Figufe 3

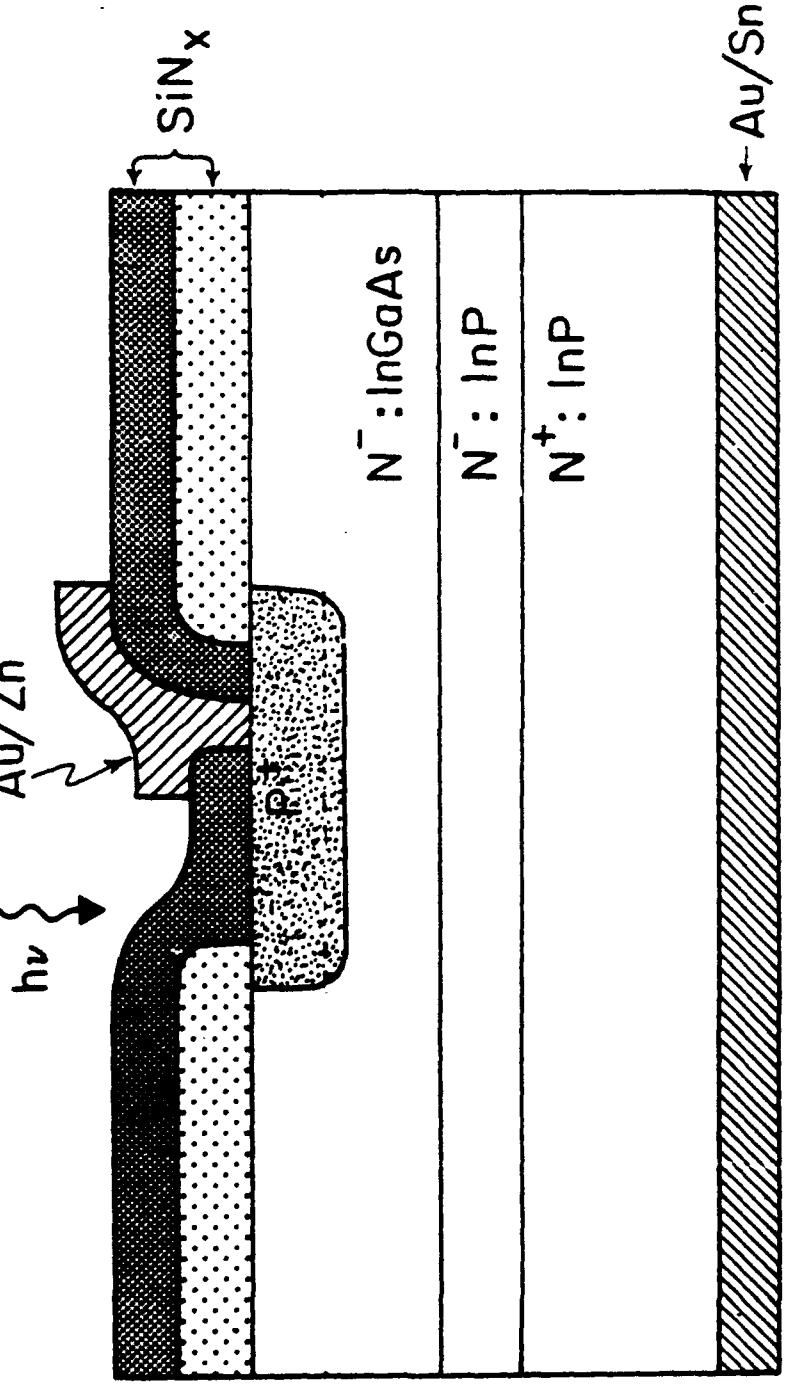


Figure 4

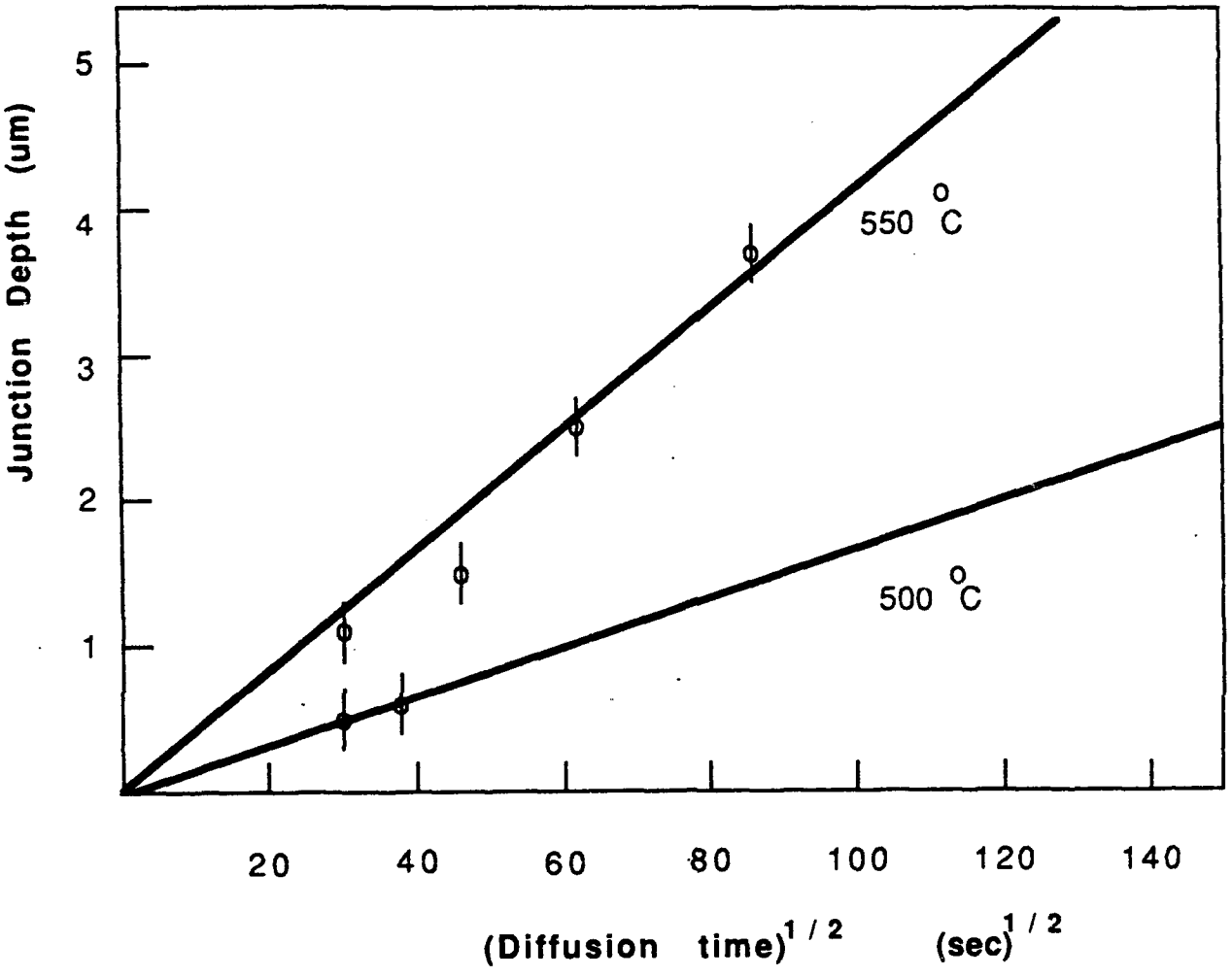

Junction Depth (um)
5
4
3
2
1
550 °C
500 °C
20
40
60
80
100
120
140
(Diffusion time)^1/2 (sec)^1/2

Figure 5

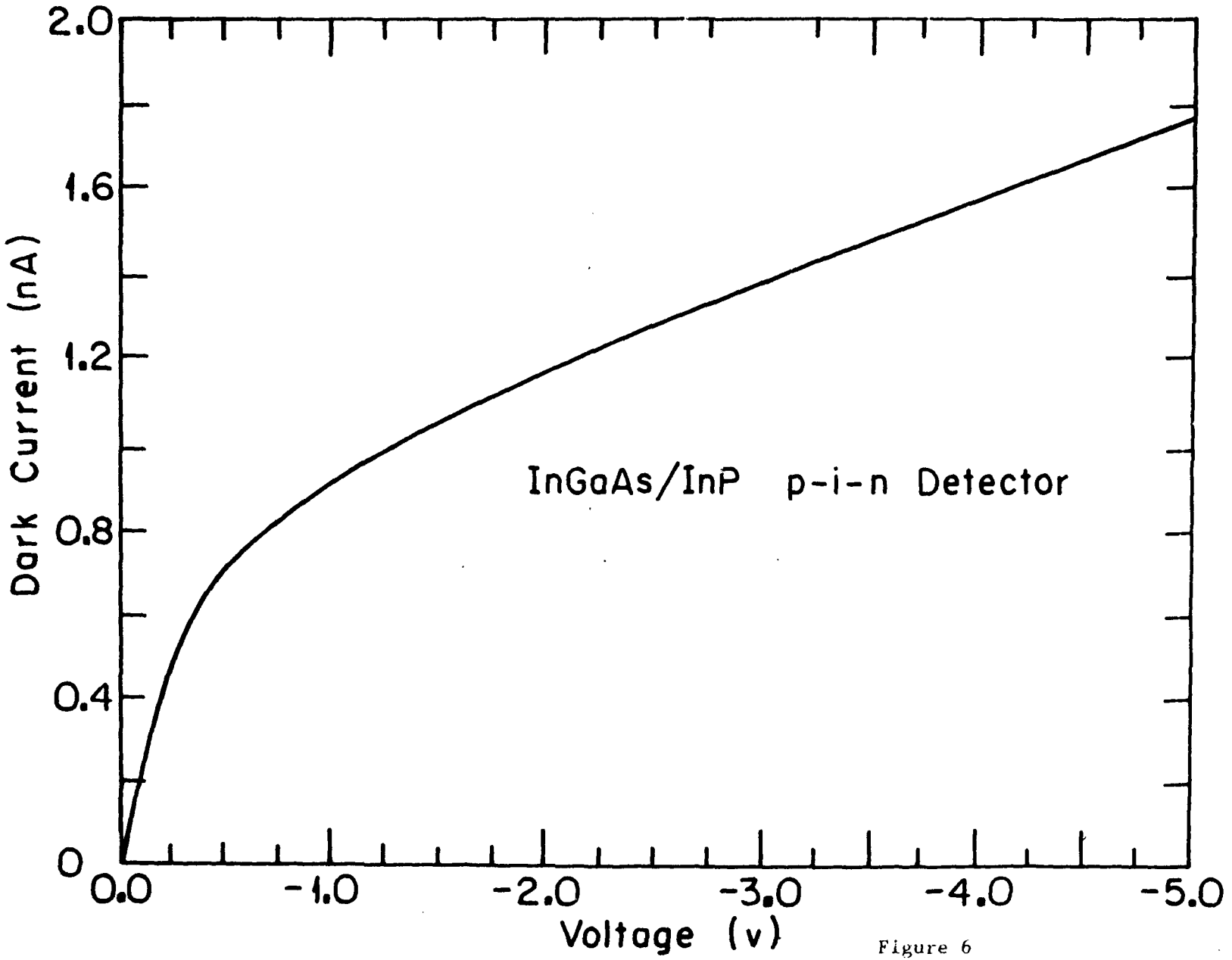

2.0
1.6
1.2
0.8
0.4
0
Dark Current (nA)
InGaAs/InP p-i-n Detector
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
Voltage (v)

Figure 6

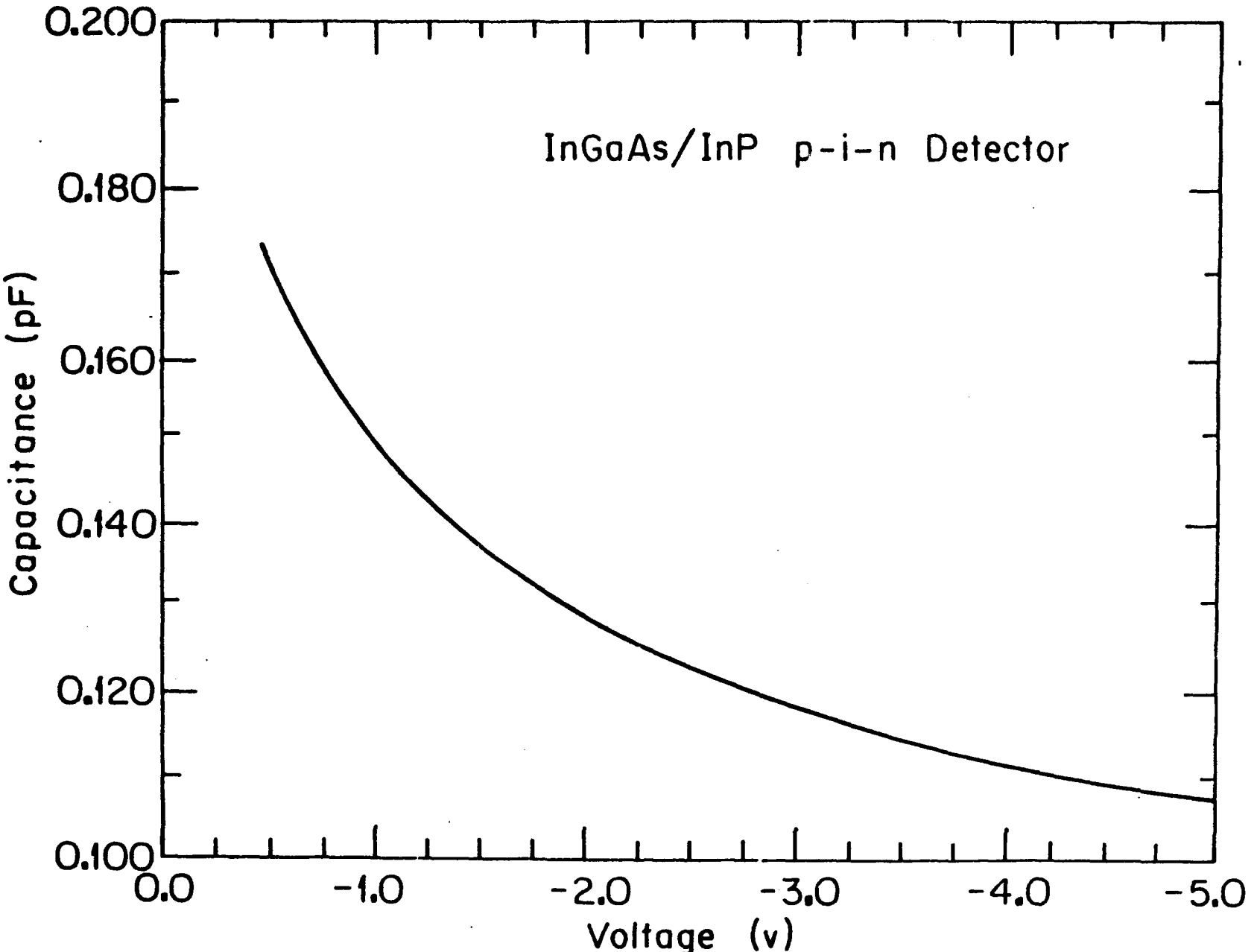

InGaAs/InP p-i-n Detector
Capacitance (pF)
0.200
0.180
0.160
0.140
0.120
0.100
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
Voltage (v)

Figure 7

discussed in the following section. For this purpose, we set up a closed-ampuole diffusion station consisting of a pump-down apparatus which is ion and vacsorb pumped to eliminate oil contamination which generally accompanies diffusion and mechanical pumps. The Zn source used was roughly 20 mg of precleaned $ZnAs_2$ loaded in a 1 cm diameter by 20 cm long quartz ampuole. The tube was then sealed and loaded into the furnace where the temperature was maintained extremely flat (to < ± 1 C over 20 cm). The diffused sample was next removed from the ampuole and the junction depth was determined by cleaving, staining an examination under a microscope. The results of this study of diffusion into InGaAs are summarized in Fig. 5. It is apparent that higher temperatures are suitable for p-i-n junction diffusion, whereas 500 C is preferable for controlling forming shallow junctions for FETs. The characteristics of the completed detector are shown in Figs. 6 and 7. Here, we observe a dark current of 1.6 nA at-5V bias, and a capacitance of 108 fF. The quantum efficiency of the top-illuminated devices (which did not have AR coating) was measured at 60%. We expect better results for devices with an InGaAsP cap layer which is interposed between the InGaAs and SiN_x materials due to the improved surface properties of InGaAsP. However, to date we have not accomplished this complicating growth step, although several InGaAsP layers have been successfully grown in our LPE system.

IV. FET Results

In order to systematically design and fabricate high performance self-aligned JFETs as that shown in Fig. 8, one of the objectives of the first year has been to generate a model which, as completely as possible, would be useful in predicting the performance of InGaAs and InP-based JFETs used

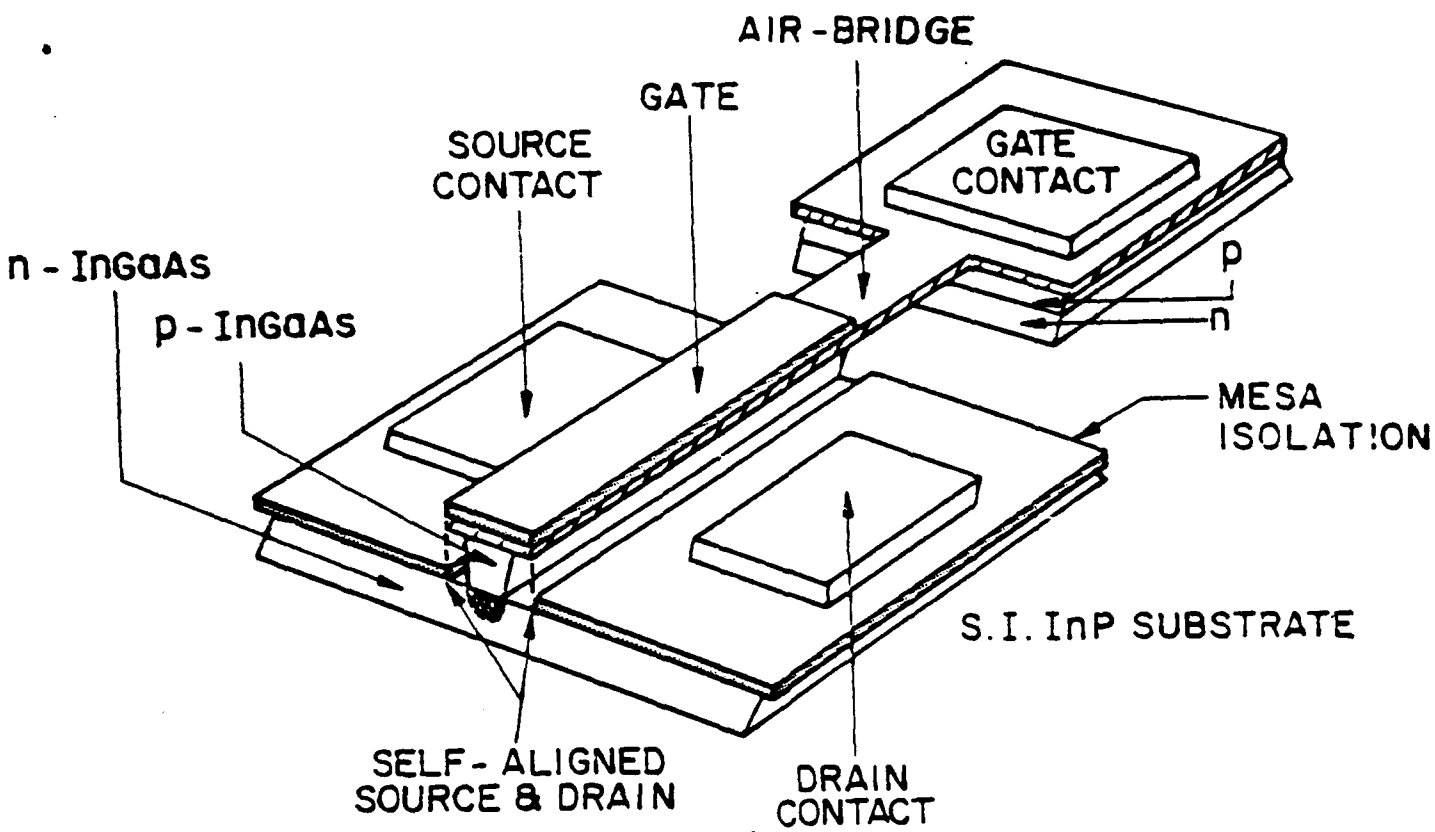

AIR-BRIDGE
GATE
SOURCE CONTACT
GATE CONTACT
n - InGaAs
p - InGaAs
p
n
MESA ISOLATION
S.I. InP SUBSTRATE
SELF-ALIGNED SOURCE & DRAIN
DRAIN CONTACT

Figure 8

in OEIC applications. This particular objective has been completely met, with the result that a model has generated, for the first time, an InGaAs and InP transistor design "recipe".

In this work, given in detail in Appendix B, we calculate, and compare with experimental results, the optimum design of InGaAs and InP JFETs for use in InP-based OEICs. For our study, we have developed an analytical model for self aligned JFETs which includes the effects of channel resistance and band-to-band tunneling. Various noise sources, such as Johnson, channel, shot, and 1/f noise, in FETs are also considered for analysing receiver sensitivity. The agreement between our calculations and experimental results for InGaAs and InP JFETs supports the validity of the model.

Figure 9 shows the external transconductance, g_m', as a function of channel doping for InGaAs, InP and GaAs JFETs. Here, we have considered a self-aligned JFET structure[4], as depicted in Fig. 8, to minimize the source- and drain-gate spacings. The plot indicates that InGaAs JFETs have the highest g_m' for low channel doping due to the high mobility (μ = 10^4 $cm^2/V\text{-}s$) and peak velocity (v_p = 2.7 x 10^7 cm/sec) of this material. However, g_m' for InGaAs JFETs is observed to decrease significantly at high channel doping due to the onset of tunneling[7]. The excessive tunneling current primarily degrades the sensitivity of devices by increasing shot noise. As a result, the optimized channel doping can be obtained by maximizing this parameter while preventing any significant increase of tunneling current. The optimized channel doping for InP is found to be larger than InGaAs due to its high breakdown electric field. However, the voltage gian and cut-off frequency for the two types of devices with optimized channel doping are approximately equivalent. Experimental data

for InGaAs (solid circles) and InP (open circles) JFETs are also shown in Fig. 8. In most cases, the experimental values for g_m' fall significantly below the calculation which is in part attributed to high source-gate resistance for non-self-aligned JFET structures such as is the case for all five InP devices shown.

In order to evaluate JFET power efficiency, we define a figure of merit as the power dissipated per transconductance (ξ'), i.e. $\xi' = I_{DS}V_{DS}/g_m'$. Here, I_{DS} is the drain current, and V_{DS} is the source-drain bias for the FET. Clearly, the highest power efficiency is obtained by minimizing ξ'. Figure 10 shows the channel doping, channel thickness, and pinch-off voltage dependence of ξ' for InGaAs and InP JFETs. In terms of this parameter, we see that InGaAs JFETs are both more efficient and more tolerant to variations in doping and thickness than are InP JFETs, implying that the former devices are more appropriate for high-density OEIC applications. Note that Fig. 10 also shows the interrelationship between the channel doping, thickness, and pinch-off voltage for optimized devices.

In Fig. 11, we show the sensitivity versus channel width and power dissipation for receivers using InGaAs and InP JFETs operating at a data rate of 1 Gb/sec. The schematic diagram of the receiver circuit is shown in the inset. For this plot, the front-end capacitance (C_{IN}) which includes photodiode and stray capacitances, is also a variable parameter. For C_{IN} = 1 pF, which is a typical value for hybrid optical receivers, sensitivity can be increased by increasing channel width (and hence g_m') at the expense of increasing power dissipation. However, for a monolithic receiver designed to minimize stray capacitance, we expect C_{IN} = 0.1 pF. In this case, channel width can be reduced to as short as 20 μm to obtain a sensitivity of -36dBm in receivers using either InGaAs or InP JFETs. Using

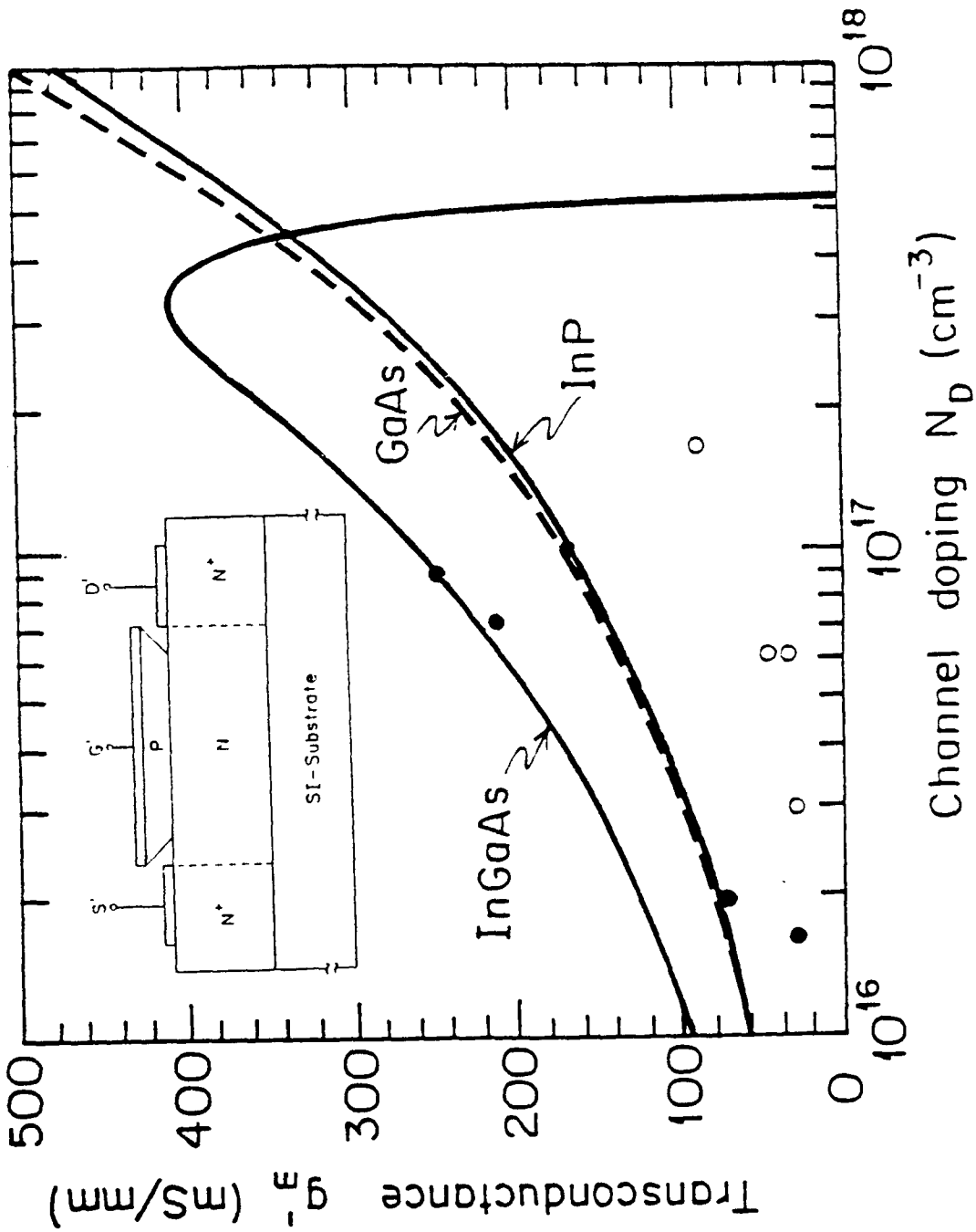

Transconductance g_m (mS/mm)
500
400
300
200
100
0
10^{16}
10^{17}
10^{18}
Channel doping N_D (cm^{-3})
GaAs
InP
InGaAs
D'
G'
S'
N+
P
N
N+
SI-Substrate

Figure 9

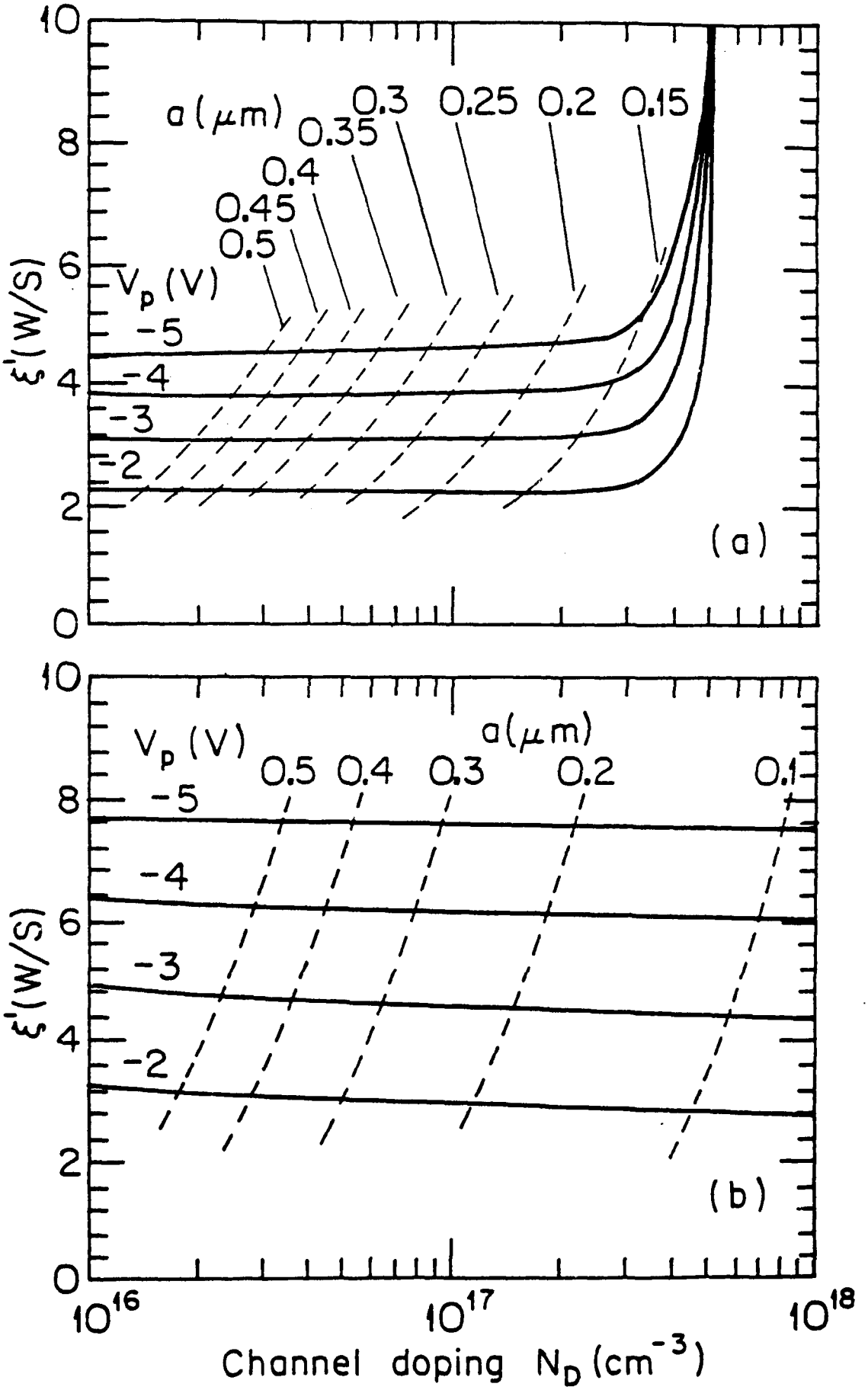

a(μm)
0.3
0.25
0.2
0.15
0.35
0.4
0.45
0.5
Vp(V)
-5
-4
-3
-2
ε'(W/S)
(a)
Vp(V)
a(μm)
0.5
0.4
0.3
0.2
0.1
-5
-4
-3
-2
(b)
10
8
6
4
2
0
10^16
10^17
10^18
Channel doping ND (cm^-3)

Figure 10

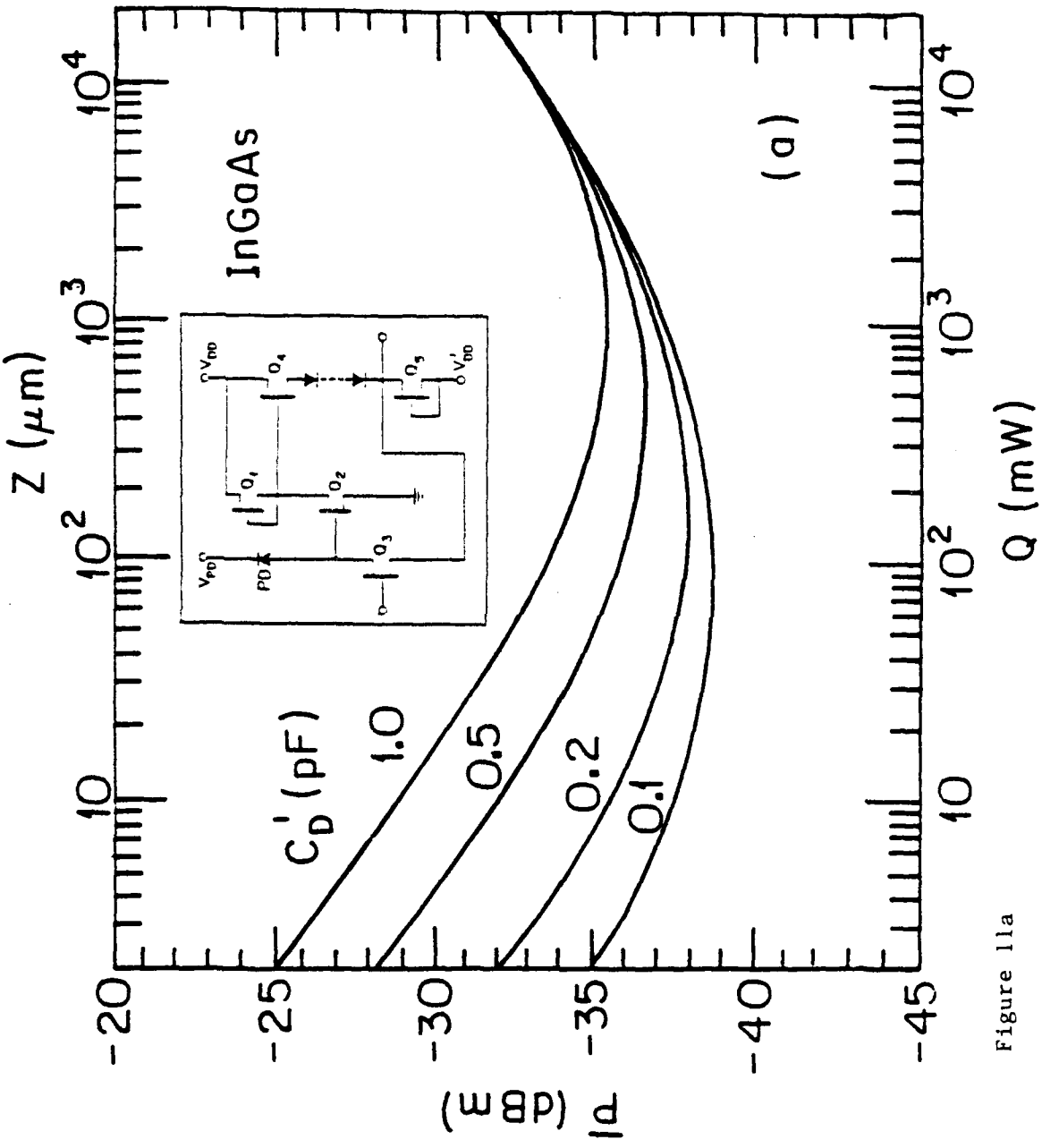

InGaAs
(a)
Z (μm)
Q (mW)
η (dBm)
C_D' (pF)
1.0
0.5
0.2
0.1
-20
-25
-30
-35
-40
-45
10
10^2
10^3
10^4

Figure 11a

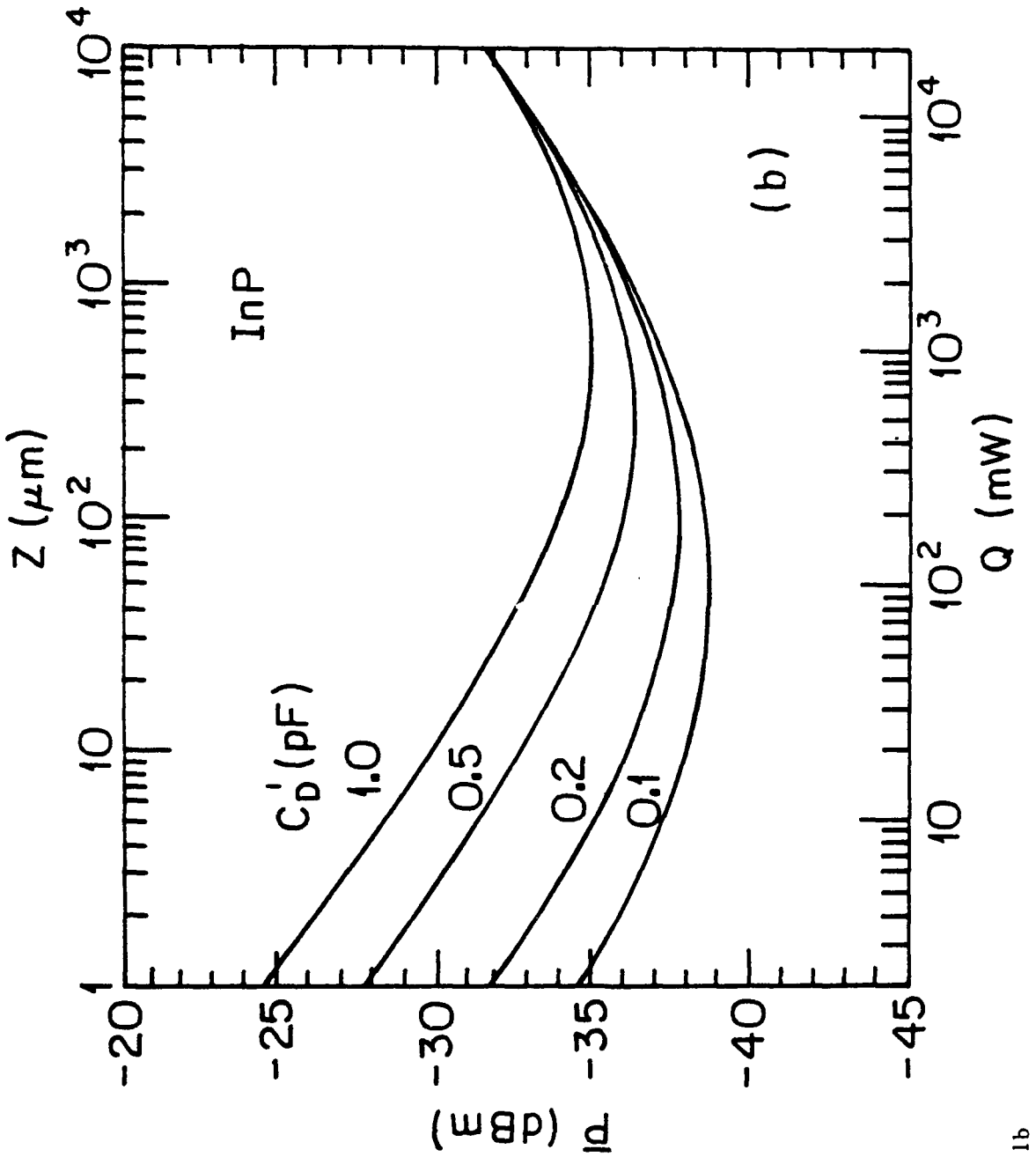

Z (μm)
InP
(b)
C_D'(pF)
1.0
0.5
0.2
0.1
η (dBm)
Q (mW)
-20
-25
-30
-35
-40
-45
1
10
10^2
10^3
10^4

Figure 11b

such small gate dimensions, InGaAs JFET circuits consume only 20 mW, while 40 mW is dissipated using InP. Such devices with small gate dimensions have a very low power dissipation, yet do not sacrifice high sensitivity. Hence, they are ideal for high density and high peformance OEICs.

In addition to device modeling which now serves as a guide to all device design, we have made some initial attempts at fabricating the self-aligned JFET structure shown in Fig. 8. As noted above, numerous growth runs for the JFET have been accomplished. In general, we require a 1 μm thick InGaAs layer for the channel, which is subsequently diffused to 0.5 μm depth using a low temperature (500 C) Zn diffusion. A channel doping of 8×10^{16} cm^{-3} is preferred, although to date we have not succeeded in achieving such a high value. This, however, should not remain a problem in subsequent work once we bring our 3rd and 4th LPE reactors into operation. In these additional furnaces, we will intentionally dope the n-type channel in order that sufficiently high doping can be achieved. We have resisted doing this in the present LPE system since we might "poison" future high purity growths needed for the p-i-n detector material.

The process steps for fabricating the JFETs have been brought under control. Hence, the gate metal (Cr-Au) is deposited, followed by a directional, undercut etch metal using Caros acid. Furthermore, successful air-bridges have also been formed. Some difficulty remains in maintaining adherence of the Au-Ge source-drain contacts, which may eventually be switched to Au-Sn contacts, depending on our progress and success with the Au-Ge metallization. However, we attribute this contact problem to excessively high humidity incurred in the photolithographic process. We note that these first FETs were partially processed in a neighboring

laboratory at USC, while the remaining steps were performed in our own laboratory. This was necessary since our own clean room facility was not completely operational due to construction needed to make long-awaited rennovations. At present, our clean room is once again completely functional, obviating humidity and dirt-related problems in current and future process runs.

Additionally, considerable control has been obtained in the p-n junction gate diffusion in that we can now reproducibly form abrupt junctions at 0.5 μm from the wafer surface (see Fig. 5). SIMS profiling of these junctions needs to be done to obtain quantitative data regarding the abruptness of the junction. At the outset of the project, we were not considering diffused junctions since grown or ion-implanted junctions were considered to be superior alternatives. However, our diffusion experiments have been extremely successful and controllable such that it may in fact prove a viable technique, pending the results of SIMS analysis.

The first successfully processed group of JFETs had a channel thickness of 1 - 1.5 μm, and a p-n junction depth of 0.6 μm. The gate width was 150 μm, and the gate was approximately 1.2 μm in length. Due to the very low doping (~5×10^{15} cm^{-3}) and excessive thickness of the channel, the JFETs exhibited saturation at approximately 2 V_{DS}, and had a concomitantly low transconductance (<10 mS/mm). However, the gate leakage was very small at 15 nA and 50 nA at a gate source voltage of -1V and -5V, respectively. These very low dark currents indicate that there is no "bridging" of the overhanging gate metal onto the source and drain contact pads, nor is there any connecting paths left beneath the gate "air bridge". Furthermore, this is the lowest gate leakage per gate width yet observed for InGaAs, self-aligned JFETs, and removes one of the primary doubts

concerning these structures -- i.e. excessive gate leakage at the junction perifery. We expect that future processing runs with our more optimized growth and processing will result in high gain, low gate leakage transistors, as expected at the outset of this project.

In one final segment of the work, we have tested various circuit designs using Si and GaAs, hybrid integrated circuits. This work is required if we are to succeed in integrating a monolithic photoreceiver in the minimum number of steps, and making a minimum number of mistakes in our mask designs. To this end, the early circuits were done at the "breadboard" level using discrete Si FETs. In more recent research, we have successfully fabricated an active load preamplifier circuit design similar to the type that we are intending to integrate using GaAs FETs. This particular circuit was mounted on a thin-film alumina substrate which was patterned and etched to accomodate the components. Our initial effort was directed at achieving extremely low receiver power dissipation. Hence, the entire, two stage preamplifier consumed roughly 10 mW, and operated at a power supply voltage of +2V and -1V. Of this power, only 2.6 mW, was dissipated in the gain stage, with the follower stage being the most power consumptive element. This situation is unavoidable if it is necessary to match the amplifier output to a 50 Ohm load -- a situation which might not be essential in all cases. Due to the low power dissipation requirement, the unequalized amplifier bit rate was held to only 45 Mb/s using NRZ format. A frequency spectrum of the receiver output using a variable frequency, sinusoidally modulated optical input is shown in Fig. 12. Future generations of this receiver will be designed to achieve higher bandwidth at the expense of power dissipation. The construction and

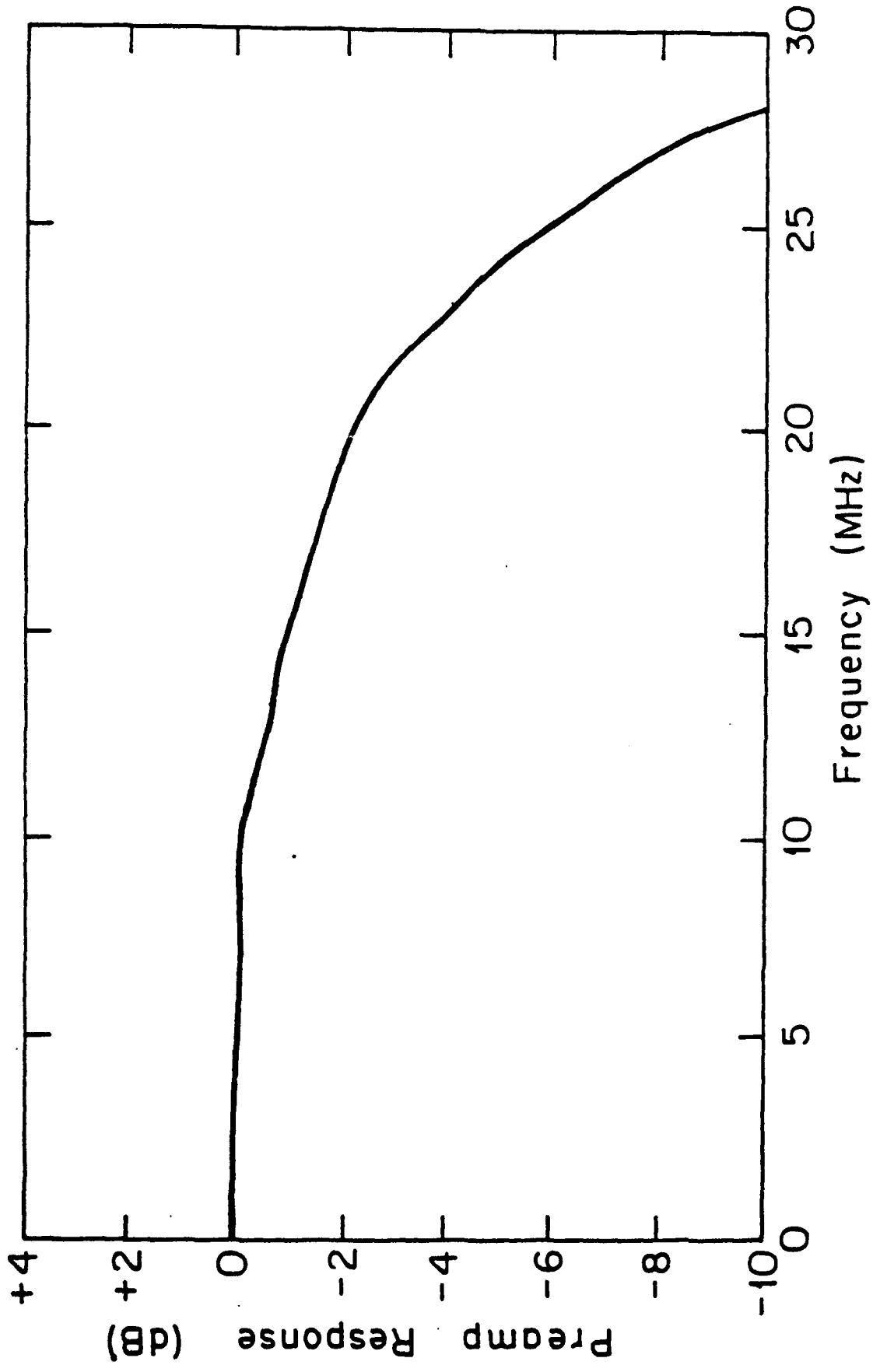


Figure 12

characterization of the preamplifier has given us important experience in the design of the circuits which soon will be committed to a mask set design for the OEIC implementation.

V. Conclusions

Although we had a small "head start" of a few months to explore the viability of JFETs for OEIC applications, this report has presented the results of the first full year of a three year program aimed at fabricating a high sensitivity, high bandwidth monolithic integrated circuit using InP-based materials. The investigation is a collaborative effort between USC and NOSC, and these results disclose only those apsects of the research done at USC. All of the goals set forth in the initial program for the first year have been accomplished in this work. We believe these accomplishments are owed in part to the continued close collaboration between USC and NOSC whereby a contuous exchange of information, resources and ideas has been allowed to occur.

We summarize the first year results as follows: We have successfully developed materials for these OEICs, although additional research needs to be done to improve material grown in wells. Due to the size of the effort at USC (one graduate student supported via NOSC), we have concentrated on other aspects of the work -- particularly in the design and demonstration of p-i-ns and FETs. To this end, the planar p-i-n technology has been well established with excellent results. Furthermore, the design criteria for InGaAs and InP JFETs have been established with the suprising result that very small gate widths (20 - 40 μm) can be tolerated with little or no degradation to device performance. This finding should result in

considerably higher yields in fabricating transistor circuits than had we needed to pursue large width transistors (100 - 200 μm) as is done at other laboratories exploring these OEICs. Initial results in fabricating self-aligned InGaAs JFETs have proven successful, although considerably improved performance is still needed for fabricating reasonable transistor circuits.

VI. Recommendations

Early in the second year of this effort, high performance JFETs need to be demonstrated. We recommend that InGaAs JFETs such as that shown in Fig. 7 be pursued as the transistor structure of choice.

However, due to the experience with InP transistors which exists with several researchers at NOSC, we suggest that InP JFETs be continued to be investigated at that laboratory. In this manner, a direct comparison between InGaAs and InP JFETs will be obtained. These results can then be used to improve our analytical models, and to give us an even clearer picture of the advantages and disadvantages inherent in each of these semiconductor materials.

The next major accomplishment expected to follow the fabrication of high quality FETs will be the design and fabrication of a monolithic transimpedance preamplifier. Hence, an early start on circuit and mask design is in order.

As in the past, the future success of this investigation depends on continued cooperation between the laboratories at USC and NOSC. Indeed, this has been an extremely rewarding aspect of the work which we are confident will continue into the remaining term of this investigation.

VII. Acknowledgements

Although the research support has been for one "full time" graduate student, in fact many students have, at one time or another made valuable contributions to the success of this work. In particular, the P.I. thanks Chia-Di Lee for materials growth and characterization, Julia J. Brown for device processing and testing, and Dennis C. W. Lo for circuit and device analysis.

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APPENDIX A

Threshold voltage drift of InP *n*-channel enhancement mode metal-insulator-semiconductor field-effect transistors

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The drift of drain-to-source current in enhancement mode InP-based metal-insulator-semiconductor field-effect transistors is analyzed. We simultaneously measure the time dependence of both the drain-to-source current (I_{DS}) and the transconductance of these devices when operated in the saturation regime. From the comparison of these long-term data, we conclude that the observed drift is caused by a variation in threshold voltage (V_T), whereas the carrier mobility in the channel appears to be independent of time. We interpret these results in terms of charge trapping in the gate insulator and infer a slow surface state density of $\gtrsim 1\times 10^{11}/\text{cm}^2$. In spite of this relatively low density of states, large scale drifts in V_T and I_{DS} are observed. Apparently, this is the first report of the long-term time dependence of the saturation transconductance and its correlation with I_{DS} drift.

Recently, there has been considerable interest in using InP and related compounds as transistor materials. The attractiveness of these materials lies primarily in their use in long-wavelength optical communications systems. Many workers have attempted to use metal-insulator-semiconductor field-effect transistors (MISFET's) as the basic electronic circuit component in this materials system. It has been almost universally found,[1-12] however, that MISFET's made by using either InP or InGaAs exhibit a variation of drain-to-source current (I_{DS}) with time when the gate-to-source bias (V_{GS}) is held constant. This phenomenon, observed to varying degrees in both enhancement and depletion mode devices, is generally referred to as drain current drift. It is apparent from the literature that there is not yet a consensus as to the source of this effect; nor has there been data available from long-term experiments which might aid in its explanation. However, it is clear that the drift in I_{DS} arises either from a variation in voltage threshold or channel mobility.[2,4-6] The former effect would arise from charge trapping in either the semiconductor bulk or at the semiconductor/insulator interface. One might also expect the carrier mobility to change because of charge trapping in the channel region, hence increasing the importance of impurity scattering of the mobile carriers.[2] Unambiguous determination of the source of the drift is essential to the development of appropriate models to explain the phenomena, as well as to its elimination as a device performance characteristic. In this letter we present data from long-term experiments which show that the time-dependent drain-to-source current is caused by a shift in threshold voltage (V_T), whereas the electron mobility appears to be largely unaffected. The experimental procedure involves the measurement of the time dependence of both $I_{DS}(t)$ and the transconductance $[g_m(t)]$ simultaneously on the same device operated in the saturation regime. We discuss measurements that correlate the time dependence of $I_{DS}(t)$ with that of $g_m(t)$ *independent of the detailed functional form of this time dependence.* This latter point is important, since $I_{DS}(t)$ displays a variety of functional forms for a given device and, furthermore, varies markedly from one device to the next.

When operated in the saturation regime, the FET drain-to-source current is given by[13]

$$I_{DS}(t)=\left(\frac{mZC_i}{L}\right)\mu_n(t)[V_{GS}-V_T(t)]^2. \qquad (1)$$

Here $\mu_n(t)$ is the electron mobility in the channel. Both $\mu_n(t)$ and $V_T(t)$ may (or may not) have the same time dependence, which is as yet undetermined. Also, m is a function of the doping concentration profile, Z is the gate width, L is the gate length, C_i is the insulator capacitance per unit area, and V_{GS} is the applied gate-to-source bias.

In past work[5,6] it has been inferred that $I_{DS}(t)$ is caused solely by a shift in V_T, as indicated in Eq. (1), on the basis of experiments in which mobility did not vary with time. For example, in the experiment of Goodnick *et al.*,[5] the drain current and mobility of special Hall geometry MISFET's, operated in the linear regime, were measured over a time of less than 40 s. The result was constant mobility with decreasing drain current. Although the results of this work suggest a variation in V_T as the sole cause of $I_{DS}(t)$, the relationship between Hall devices measured in the linear regime and FET's operated in the saturation regime is unclear. The correspondence of the time dependence of the mobilities in these two regimes, which might be expected to be influenced by carrier scattering from trapped charges, is not obvious. Indeed, in our own experiments we have found that while the mobility appears time independent in devices operated in the saturation mode, this is not found to be generally true for devices operated in the linear regime.

In another experiment, Kobayashi *et al.*[6] used a pulsed gate-to-source voltage (V_{GS}) measurement where the maximum pulse width was 1 s. From the resultant linear relationship between $I_{DS}^{1/2}$ and V_{GS}, it was concluded that mobility was constant in time [cf. Eq. (1)]. Such a pulsed experiment, however, was used to measure only the short-term

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behavior of the device, and therefore its correspondence to the long-term behavior of the drain current is ambiguous. Additionally, the dc drift and pulsed measurement in this paper do not appear to be consistent.

The time-dependent device characteristics of interest in this work are $I_{DS}(t)$ and transconductance $g_m(t)$. Now $g_m(t)$ in the saturation regime is given by[1]

$$g_m(t) = 2\left(\frac{mZC}{L}\right)\mu_n(t)\left[V_{GS} - V_T(t)\right]. \tag{2}$$

Comparing Eqs. (1) and (2) gives

$$\frac{I_{DS}(t)}{I_{DS}(t_0)} = \left(\frac{g_m(t)}{g_m(t_0)}\right)^n, \tag{3}$$

for some value n representing the contribution of mobility and threshold voltage to $I_{DS}(t)$ and $g_m(t)$. Also, t_0 is an arbitrary time at which the experiment begins. The value of n is well defined for the following two cases: If the mobility is independent of time so that the entire time dependence of the drain current is due to temporal variations of the threshold voltage, we expect a value of $n = 2$. In the other case, if the threshold voltage is constant, and $I_{DS}(t)$ depends solely on the time dependence of the mobility, then we expect a value of $n = 1$. Values of n different from 1 or 2 might indicate an ambiguous mixture of mobility and threshold voltage effects. From the experiment of measuring $I_{DS}(t)$ and $g_m(t)$ simultaneously for the same device, one can calculate the value of n and therefore infer the source of the time dependence of these parameters.

The MISFET's used in our work have a SiO_2 insulator deposited onto semi-insulating InP with an aluminum gate of dimensions $Z = 400\ \mu$m and $L = 4\ \mu$m. The processing sequence and geometry have been described previously.[7] The electron concentration in the substrate was mid to high $10^8/cm^3$, and the electron mobility was 2000 $cm^2/(V\,s)$. The gate dielectric was deposited by indirect plasma enhanced chemical vapor deposition. A partial pressure of phosphorus was supplied during the initial stages of dielectric deposition. The phosphorus was introduced in different ways for the two devices reported in this letter. A mixture of 10% phosphine in argon was used for device *A*. In the case of device *B*, solid red phosphorus was used.

In Fig. 1, I_{DS} is plotted for devices *A* and *B* as a function of drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}).

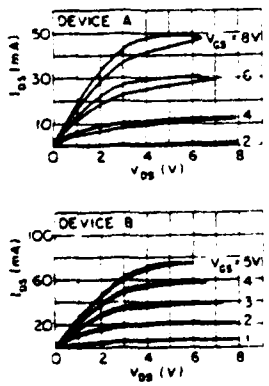

FIG. 1. Drain-to-source current (I_{DS}) as a function of drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}) for devices *A* and *B*.

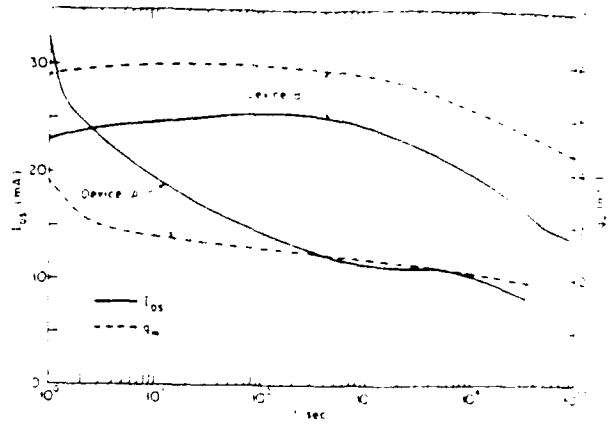

FIG. 2. Drain-to-source current (solid lines) and transconductance (dashed lines) in the saturation regime as a function of time for devices *A* and *B*.

(V_{GS}). Here V_{GS} is varied in these plots by 2 V/step for device *A* and 1 V/step for *B*. The hysteresis in I_{DS} indicates that the number of free carriers in the channel of the device is a function of the direction of applied bias (e.g., whether it is increasing or decreasing). It should be kept in mind that the hysteresis is a result of relatively fast trapping and emission of charges, and hence are not necessarily the states that are studied in long-term drift experiments such as those presented here.

In Fig. 2, $I_{DS}(t)$ and $g_m(t)$ are plotted for the two devices under study for a time period of $1 \le t < 10^5$ s. The experiment was performed by applying a constant drain potential V_{DS}, whereas the gate potential V_{GS} consisted of a small ac voltage superimposed on a much larger constant dc offset. The ac voltage was used to determine g_m, whereas the dc biases were used to set the quiescent point and simultaneously to determine I_{DS}. All the measurements were made at room temperature. It can be seen from Fig. 2 that device *A* exhibits a monotonic decrease in I_{DS}, whereas *B* shows an initial increase in I_{DS} followed by a long-term decrease.

The data of Fig. 2 are replotted in Fig. 3 to show $I_{DS}(t)$ as a function of $g_m(t)$. Each point on this plot represents the

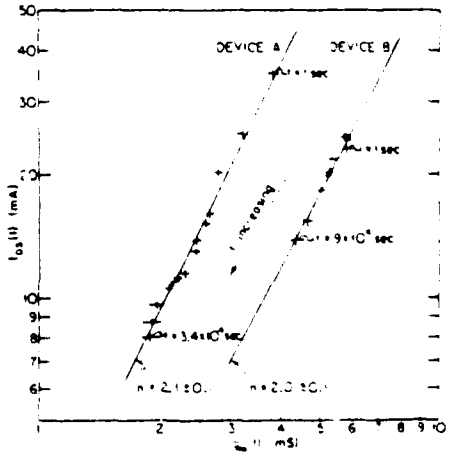

FIG. 3. Time-dependent drain-to-source current [$I_{DS}(t)$] as a function of the time-dependent transconductance [$g_m(t)$] of devices *A* and *B* operated in the saturation regime. Each point represents values of I_{DS} and g_m at the same point in time. A least-squares fit to the data results in the n values shown.

A-2

values of I_{DS} and g_m at the same point in time. From a least-squares fit to these data, we find that for device A, $n = 2.1 \pm 0.1$, and for device B, $n = 2.0 \pm 0.1$ [cf. Eq. (3)]. Thus, to within experimental error, $n = 2$, from which we can infer that the I_{DS} drift of both devices is due solely to the time dependence of V_T. This conclusion is independent of the details of the time dependence of I_{DS}, which are different for devices A and B (Fig. 2). It also appears to be independent of the gate fabrication processes used.

Our conclusion that V_T varies with time is interpreted as follows. The threshold voltage is expressed by using[13]

$$V_T(t) = 2\phi_B + \frac{(4\epsilon_s q N_a \phi_B)^{1/2}}{C_i} + \frac{qN_{ss}(t)}{C_i}. \quad (4)$$

Here ϕ_B is the built-in potential, ϵ_s is the relative semiconductor permittivity, N_a is the substrate doping, q is the electronic charge, and N_{ss} is the number of electrons trapped in the insulator per unit area. All but N_{ss} are parameters fixed by the materials and geometric properties of the device. Therefore, the fact that the threshold voltage varies indicates that N_{ss} is a function of time. The change in V_T (or ΔV_T) and hence the change in N_{ss} can be calculated from the data in Figs. 2 and 3. It is found that $\Delta V_T = 1.5$ V, from which we infer $N_{ss} = 2.3 \times 10^{11}/\text{cm}^2$ for device A, and $\Delta V_T = 0.8$ V, implying $N_{ss} = 1.3 \times 10^{11}/\text{cm}^2$ for B. Note that we expect the total number of interface traps to be somewhat larger than the number of trapped charges. As the experiment time is increased to allow for the trapping of a larger number of charges at the interface, we expect N_{ss} to approach the total number of slow defect states. Nevertheless, these values for N_{ss} are consistent with values for high-quality interfaces that typically have total defect states densities of $\gtrsim 10^{11}/\text{cm}^2$.[7,14]

In summary, the time-dependent drifts of I_{DS} and g_m in InP-based enhancement mode MISFET's operated in the saturation regime were measured and analyzed. Apparently, this is the first report of measurement of long-term g_m data and their correlation to I_{DS}. It was shown that the quadratic dependence between I_{DS} and g_m implies that the drift of these two parameters is due to a variation in threshold voltage as opposed to electron mobility. This result is interpreted as due to charge trapping and emission in the gate insulator. Physical insight into the mechanism of drain current drift provided by this experiment can be the basis for further work in modeling the drift phenomenon in InP based MISFET structures.

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APPENDIX B

Submitted to J. of Lightwave Technology

Performance of $In_{0.53}Ga_{0.47}As$ and InP Junction Field-Effect Transistors for Optoelectronic Integrated Circuits. I. Device Analysis

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Abstract

We have developed an analytical model to study $In_{0.53}Ga_{0.47}As$ and InP junction field effect transistors (JFETs) for use in InP-based optoelectronic integrated circuits (OEICs). This model includes the effects of channel resistance and band-to-band tunneling. The agreement between the calculations and experimental results reported for $In_{0.53}Ga_{0.47}As$ and InP JFETs supports the validity of the model. In addition, we discuss the optimum design for $In_{0.53}Ga_{0.47}As$ and InP JFETs, and compare their performance quantitatively. In order to prevent device performance from being degraded by the effects of tunneling, the optimum channel dopings of $In_{0.53}Ga_{0.47}As$ and InP JFETs are found to be $7x10^{16}$ and $5x10^{17}$ cm^{-3}, respectively. Also, for $In_{0.53}Ga_{0.47}As$ JFETs not operated in the tunneling regime, these devices show at least a 40% higher efficiency than InP JFETs in terms of the power dissipated per transconductance. By this and other criteria, we conclude that $In_{0.53}Ga_{0.47}As$ JFETs are well suited for very high density monolithic integration, where power efficiency must be high.

Performance of $In_{0.53}Ga_{0.47}As$ and InP Junction Field-Effect Transistors for Optoelectronic Integrated Circuits. I. Device Analysis

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I. Introduction

The goal of optoelectronic integrated circuits (OEICs) is to monolithically integrate photonic devices--such as lasers, modulators, and photodetectors--together with their associated electronic circuitry in efforts to increase device functionality and performance at a reduced cost [1]. In particular, considerable research has focussed on integrated devices utilizing GaAs-based alloys due to the mature state of their electronic technology. Sophisticated GaAs-based OEICs such as a four-channel transmitter array [2], as well as a four-channel optical receiver array [3] have been successfully demonstrated. However, because of interest in optical transmission in the wavelength range between 1.3 and 1.55 μm, InP-based alloys have also attracted attention for OEIC applications.

Unfortunately, InP-based transistor technology is still in its infancy, although several $In_{0.53}Ga_{0.47}As$ (hereafter referred to as InGaAs) and InP field-effect transistor structures have already been investigated. Unlike the case of GaAs, the low Schottky barrier heights formed on InGaAs

and InP prohibit the fabrication of high performance metal-semiconductor field-effect transistors (MESFETs) [4]. In addition, the poor quality of InP/insulator interfaces induces drain-current drift leading to unstable metal-insulator-semiconductor field-effect transistor (MISFET) characteristics [5,6]. For these reasons, junction field-effect transistors (JFETs) have been widely pursued for use in InP-based OEIC applications.

Many promising results for both InGaAs and InP JFETs have been reported. Cheng, et al. [7] and Wake, et al. [8] have demonstrated a self-aligned InGaAs JFET grown on semi-insulating InP substrates. Transconductances of such InGaAs JFETs as high as 210 mS/mm have been obtained [9]. In addition, Boos, et al. [10] and Kim, et al. [11] have fabricated planar InP JFETs, and obtained transconductances of roughly 100 mS/mm. Thus, many research groups have studied InGaAs or InP JFETs for use in OEICs, but whether the InGaAs or InP JFET is more appropriate for these applications has heretofore not been considered in detail.

Along with device development, device models have also been conceived as design tools for optimization. The analytical two-region model, developed by Grebene and Ghandi [12], and extensively modified by Pucel, et al. [13], has been successfully applied to silicon JFETs and GaAs MESFETs, and has recently been modified by Hill to describe InGaAs and InP MISFETs [14]. In this paper we apply, for the first time, the two-region model to InGaAs and InP JFETs, and investigate the influence of electron transport properties, such as mobility and peak velocity, on device performance. Since electron band-to-band tunneling occurs in narrow band gap and small effective mass semiconductors such as InGaAs [15], we also include this

effect in our model. It is the purpose of this paper to determine the expected performance and design criteria of InGaAs and InP JFETs for use in OEIC applications.

The paper is organized as follows: In Sec. II we present the extended JFET model, discussing several characteristic parameters such as transconductance, output resistance, and gate-source capacitance for InGaAs and InP JFETs. In Sec. III, we discuss the optimization of device performance, i.e., power dissipation and voltage gain of devices for use in OEICs. Finally, in Sec.IV, we present our conclusions. In a subsequent paper (Paper II) we apply the results of this study to analyze the performance of an archetype optoelectronic integrated circuit--i.e. an optical receiver.

II. Model Description

We consider the self-aligned JFET structure [7,8] shown in Fig.1(a), which consists of p-n epitaxial layers grown on a semi-insulating (SI) InP substrate. When the JFET is operated in saturation, the channel of the device can be divided into two regions along the direction of current flow. At the interface between the two regions where $x = L_1$, the electron reaches its peak velocity. In the region near the source ($0 \leq x \leq L_1$), the electron mobility is assumed constant such that the electron drift velocity varies linearly with the electric field. In the drain region ($L_1 \leq x \leq L$), any change in channel width, $y(x)$, or electron drift velocity due to increasing electric field, is compensated by a change in electron density to assure current continuity. An increase in drain voltage increases the longitudinal electric field; hence, electrons reach peak velocity at a

position closer to the source, thereby reducing the magnitude of L_1. The depletion width (W_c) at $x = L_1$ is a function of the drain and gate voltages. Both L_1 and W_c can be obtained numerically, as described in detail elsewhere [12,13,16]. Once L_1 and W_c are known, the characteristic parameters of the transistor such as drain current, transconductance, gate-source capacitance, and output resistance can be obtained [13].

In our treatment, the model is further modified to include the parasitic source and drain resistances consisting of the contact (R_c) and bulk (R_{SG}, R_{DG}) resistances of source-gate and drain-gate regions, as indicated in Fig.1(a). The contact resistance is given by the transmission-line model [17], viz:

$$R_C = (\rho_c R_S)^{1/2}/Z, \qquad (1)$$

where ρ_c is the contact resistivity, Z is the gate width, and R_S is the sheet resistance given by $R_S = 1/(qN_D\mu a)$ for n-type semiconductors. Here q is the electronic charge, N_D is the donor concentration, μ is the electron mobility, and a is the channel thickness. The sheet resistance can be reduced by modifying the self-aligned structure. For example, in a confined-area-channel JFET (CAC-JFET) structure such as that shown in Fig.1(b), high source and drain doping is used to reduce R_S, as well as to confine the channel volume. This can be achieved using self-aligned ion implantation of the contacts. Using this modified structure, a reduction in the contact resistances is expected.

Next, R_{SG} and R_{DG} can be obtained using:

$$R_{SG} = L_{SG}/(qN_D\mu aZ), \qquad (2)$$

$$R_{DG} = L_{DG}/(qN_D\mu aZ), \qquad (3)$$

where L_{DG} and L_{SG} are the drain-gate and source-gate spacings, respectively. In a self-aligned JFET, L_{SG} and L_{DG} can be reduced to about 0.5μm [7,8]. Since InP has a smaller electron mobility than InGaAs (see Table I), the bulk resistance is about 3 to 4 times larger for InP than for InGaAs for such self-aligned devices. As will be discussed below, this difference in bulk resistance has a significant effect on the corresponding device performance.

To test the validity of the two region model, we have used it to fit the experimental drain current characteristics of both InGaAs and InP JFETs. The results of these fits are shown in Fig.2, where the data (shown as solid circles) are taken from Cheng and co-workers [18] for a L = 1 μm InGaAs JFET (Fig.2(a)), and from Boos, et al. [10] for a 2-μm InP device (Fig.2(b)). It is observed that the fits are indeed accurate for the InP device over the entire range of biases used in the experiment. Similarly convincing fits are obtained for InGaAs, particularly for a gate-source voltage of $V_{GS} > -0.8$ V. The saturation voltage, V_{DSAT}, is indicated by the dashed lines in the plot, and corresponds to the applied drain voltage when the electrons in the channel reach peak velocity under the gate. Taking into account the different device gate lengths, we find that V_{DSAT} is at least 0.5 V smaller for InGaAs than for InP JFETs due to differences in electron mobilities and critical electric fields for these two materials. Here, the critical electric field corresponds to the field at which an electron reaches peak velocity. As will be discussed below, this difference in V_{DSAT} between these materials also has a significant effect on their overall performance in high density OEIC applications.

For a transistor operating under strong saturation ($L_1 \simeq 0$), the transconductance can be approximated by

$$g_m \simeq \epsilon_s v_p Z/W_c \simeq v_p Z(\epsilon_s q N_D/[2(V_{bi} - V_{GS})])^{1/2}, \quad (4)$$

where ϵ_s is the permittivity of the semiconductor, and V_{bi} is the built-in potential given by $qV_{bi} = kT ln(N_A N_D/n_i^2)$. Here k is the Boltzmann constant, T is the junction temperature, n_i is the intrinsic carrier concentration, and N_A is the acceptor concentration. Including the effects of channel resistance, the external g_m' is given by

$$g_m' = g_m/(1+R_{SG}g_m). \quad (5)$$

To achieve high transconductance, it is necessary to increase the channel doping to values well beyond those used in the FETs in Fig.2 (where $N_D = 2.0 \times 10^{16}$ cm^{-3} and 1.5×10^{17} cm^{-3} for the InGaAs and InP devices, respectively). However, it has been shown that such an increase in channel doping can result in increased gate leakage due to the onset of band-to-band tunneling in the reverse-biased drain-gate p-n junction [19,20]. The nearly exponential increase in gate leakage current with applied voltage, which is a characteristic of tunneling, can strongly degrade the transconductance, output resistance, and noise performance of the devices, and thus it must be taken into consideration in the design of such FETs. The gate leakage current consists of contributions from surface leakage, diffusion, generation-recombination, and tunneling. Here the tunneling current, which dominates at high electric fields, can be described by [19,20]:

$$I_{tun} = \gamma A \exp[(-2\pi\alpha m^{*1/2} E_g^{3/2})/(qhF_m)], \quad (6)$$

where A is the junction area, m^* is the electron effective mass, E_g is the energy gap, h is Planck constant, and F_m is the maximum junction electric

field. Assuming a one-sided abrupt p^+-n junction at the gate, F_m is given by:

$$F_m = [2q N_D(V_{DS} + V_{bi} - V_{GS})/\epsilon_s]^{1/2}. \quad (7)$$

In Eq.(6), α is a factor that depends on the detailed shape of the tunneling barrier. Assuming a parabolic potential barrier for band-to-band processes, it has been shown that $\alpha \simeq 1.11$ [16]. The prefactor, γ, is given by [19,20]:

$$\gamma = (2m^*/E_g)^{1/2}[q^3F_m(V_{DS} + V_{bi} - V_{GS})]/h^2. \quad (8)$$

According to Eq.(6), materials with a small band gap or electron effective mass, such as InGaAs, will have a relatively large tunneling current contribution. This can be seen from Fig.3, which shows the bias voltage (indicated as dashed lines) at which the tunneling current density reaches 1 mA/cm^2 as a function of carrier concentration for InGaAs and InP p^+-n abrupt junctions. The figure indicates that this voltage for InGaAs is about one order of magnitude smaller than for InP. The avalanche breakdown voltage (indicated by solid lines) is determined using the empirical equation [16]:

$$V_B = 60(E_g/1.11)^{3/2}(N_B/10^{16})^{-3/4} \quad (8)$$

is also shown in Fig. 3 for these two materials. A comparison of these curves shows that tunneling dominates over avalanche breakdown at $N_D > 7\times10^{16}$ cm^{-3} for InP, and all values of N_D considered for InGaAs. Note that these results are consistent with data obtained for InP and InGaAs p-n junction devices [21,22].

Excessive tunneling current results in an increase of saturation drain current, such that both the transconductance and output resistance of the FET are degraded. The decrease of transconductance from its value in the

absence of tunneling, Δg_m, can be found by differentiating Eq.(6) with respect to V_{GS} to obtain

$$\Delta g_m = -[1.5/(V_{DS} + V_{bi} - V_{GS}) + (2\pi\alpha m^{*1/2} E_g^{3/2})/(qhF_m^2 W_t)] I_{tun}, \quad (9)$$

where W_t is the depletion width given by $W_t = [2\epsilon_s(V_{DS} + V_{bi} - V_{GS})/qN_D]^{1/2}$.

From the above analysis, the exponential increase in I_{tun} with V_{DS} and V_{GS} leads to a proportionate decrease in g_m. Figure 4 shows the degradation of g_m due to the onset of tunneling in an InGaAs JFET with a 1 μm long channel doped to 1.5×10^{17} cm^{-3}. The solid lines indicate the values of g_m if the effect of tunneling is not considered, while the dashed lines indicate the value of transconductance in the presence of tunneling.

In Fig.5, we plot g_m' at $V_{GS} = 0$ versus N_D for InGaAs and InP JFETs with 1 μm long channels. Materials parameters used in this calculation are given in Table I. Also, g_m' for equivalent GaAs JFETs (using $\mu = 7500$ $cm^2/V\text{-}s$, and $v_p = 2.1 \times 10^7$ cm/s) are also shown for comparison. The InGaAs JFETs show a higher g_m' than equivalent InP and GaAs JFETs for low values of N_D due to its low value of R_{SG} as well as the high peak velocity and narrow band gap (and hence small V_{bi}). On the other hand, InP JFETs have a calculated g_m' slightly less than GaAs JFETs due to the relatively large value of R_{SG} of the former compound. Note also that the g_m' for InGaAs decreases significantly for $N_D > 3.0 \times 10^{17} cm^{-3}$ due to the onset of tunneling.

In Table II we present data on a few recent results reported for InGaAs and InP JFETs. The data points of g_m' for InGaAs (solid circles)

and InP (open circles) JFETs are also shown in Fig.5. In plotting these data points, we assume that the transistor is operated in strong saturation, in which case g_m (and hence g_m') is independent of gate length (see Eq. (4)). Notice that in most cases the experimental values for g_m' fall significantly below the calculated values, which is in part attributed to high R_{SG} for non-self-aligned JFET structures such as is the case for all five InP devices shown. Another reason for the discrepancy is the existence of the parasitic contact resistances which are neglected in our calculation. Nevertheless, these curves indicate an upper limit to ideal device performance which has, in fact, been achieved for a few InGaAs JFETs such as that shown in Fig.1a. A second conclusion to be drawn from the figure is that, in general, the performance of InGaAs JFETs has far exceeded that of InP devices suggesting that it is considerably easier to minimize parasitic resistances in the former semiconductor.

As discussed previously, the tunneling current increases with channel doping and bias. Thus, to avoid any increase of gate leakage which rapidly degrades device performance (such as by increasing the shot noise in optical receivers, as discussed in Paper II), the tunneling current should be less than the sum of other gate leakage and photodiode dark current sources. Assuming these other current sources can be maintained at $\leq$ 10 nA, we find that the channel doping of InGaAs JFETs must be kept below 7.0×10^{16} cm^{-3}, and less than 5.0×10^{17}cm^{-3} for InP JFETs. From Fig.5, these maximum channel dopings results in a maximum transconductance of 220 mS/mm for InGaAs JFETs with 1 μm channel length, and 340 mS/mm for equivalent InP JFETs.

An additional parameter needed to quantify the performance of JFET-based circuits is the output resistance, r_o. Under saturation conditions ($L_1 < L$), the output resistance can be approximated by [13]:

$$r_o \simeq (1/v_p Z)[2(V_{bi} - V_{GS})/(\epsilon_s q N_D)]^{1/2} \cosh[\pi(L - L_1)/2a]. \qquad (10)$$

Equation (10) becomes invalid when L_1 approaches zero, and thus it is not applicable for modeling devices under strong saturation. In this treatment, the channel-widening effect due to the influence of an interfacial barrier between the active layer and the semi-insulating substrate [29] has been neglected. In some cases, however, this is an important mechanism largely responsible for the continuous increase of the drain current after saturation. Therefore, the model generally yields values of r_o higher than experimentally obtained. Nevertheless, Eq.(10), gives a qualitative understanding of how r_o scales with other FET design parameters. Note that r_o is also decreased with the onset of tunneling. Following the treatment leading to Eq. (9) for g_m, we obtain for the change of r_o (or Δr_o) with tunneling:

$$(\Delta r_o)^{-1} = \Delta g_d = \partial I_{tun}/\partial V_{DS} = -\Delta g_m, \qquad (11)$$

where g_d is the channel output conductance.

Figure 6 shows the output resistance versus channel doping for InGaAs and InP JFETs at a bias point of $V_{GS} = 0$ and $V_{DS} = V_{DSAT} + 1.2$ V, with pinch-off voltage as a parameter. Here, the pinch-off voltage is equal to the gate voltage when $I_{DS} = 0$, and is given by $V_p = -qN_D a^2/(2\epsilon_s) + V_{bi}$. The additional 1.2 V is assumed to ensure sufficient FET saturation even in the presence of large a.c. voltage swings in V_{GS}, while keeping V_{DS} small

to avoid tunneling or avalanche breakdown. Also, $V_{GS} = 0$ is chosen to obtain maximum g_m'. These figures indicate that InGaAs JFETs have higher values of r_o (by a factor of two) than InP JFETs which results from the smaller L_I in InGaAs than in an equivalent InP JFET at a given bias point. This is attributed to higher critical electric field in InP than in InGaAs. However, as tunneling becomes significant at $N_D > 2x10^{17}cm^{-3}$ for the InGaAs transistors, the values of r_o are degraded rapidly, as expected from Eq. (11).

Finally, for high-speed applications, gate-source capacitance needs to be minimized. Unfortunately, either increasing the channel width or channel doping to achieve a high transconductance will also increase the gate-source capacitance (C_{GS}). Under strong saturation conditions, C_{GS} can be approximated by:

$$C_{GS} \simeq \epsilon_s ZL/W_c \sim ZL[\epsilon_s qN_D/2(V_{bi} - V_{GS})]^{1/2}. \quad (12)$$

Both g_m and C_{GS} depend on channel doping or, more specifically, the donor concentration near the p-n junction, and have little dependence on channel thickness. Combining Eqs.(5) and (12), we obtain the cut-off frequency for the JFET, viz:

$$f_T = g_m'/(2\pi C_{GS}) = v_p/(2\pi L) = 1/(2\pi\tau_r), \quad (13)$$

which only depends on v_p or τ_r. Here τ_r is the effective gate transit time of an electron. Due to the similarity in v_p for InGaAs and InP as listed in Table I, f_T is only weakly material dependent. Typically, $f_T \simeq 35$ GHz for these FETs assuming $L = 1$ μm.

III. Design Considerations for JFETs

Based on this extended model, we consider in the following discussion the optimization of an "intrinsic" device where only bulk resistances (R_{SG} and R_{DG}) are taken into account. Note that the contact resistance is often the major contributor to the parasitic FET resistances, and that the ratio of contact to bulk resistance is equal to $(\rho_c/R_s)^{1/2}/L_{SG}$. Typical values for ρ_c are approximately 4×10^{-6}, 1×10^{-5}, and 1×10^{-5} Ω-cm^2 for InGaAs, GaAs, and InP, respectively, although they can vary considerably from wafer to wafer due to their strong process dependence [30,31,32]. The specific contact resistances obtained from Eq.(1) are, therefore, from 2 to 4 times larger than R_{SG} for the self-aligned JFETs. However, R_c is presumably reducible through proper device fabrication, and hence will be neglected in the following treatment.

In order to evaluate overall device performance, we define the transistor figure of merit as the ratio of the power dissipation to the transconductance of a transistor, i.e.,

$$\xi' = I_{DS}V_{DS}/g_m'. \tag{14}$$

Here, I_{DS} is the drain-source current taken at a bias of $V_{GS} = 0$ and $V_{DS} = V_{DSAT} + 1.2$ V. Clearly, the smaller the value of ξ', the higher the power efficiency. Figure 7 shows ξ' for InGaAs and InP JFETs at the specified bias point versus channel doping, with channel thickness and pinch-off voltage as parameters. Note that ξ' for InGaAs JFETs increases dramatically at large N_D due to the onset of tunneling (Fig.7a). When these devices are not operated in tunneling regime, however, ξ' shows only a small dependence on N_D, which results since $I_{DS}V_{DS}$ at a fixed V_p has the same dependence on N_D [$\propto (N_D)^{1/2}$] as does g_m'. Also ξ' is reduced as V_p

increases (i.e., less negative). However, we require that $V_p \leq -2V$ to ensure that devices do not operate near the pinch-off region.

A comparison of Figs.7(a) and (b) shows that the value of ξ' for InP JFETs is more sensitive to variarions in channel doping and thickness than for InGaAs JFETs. For example, in varying N_D from $1x10^{17}$ to $2x10^{17}$ cm^{-3}, ξ' for InGaAs JFETs also doubles, while for InP devices, ξ' increases by a factor of four. This implies that achieving device performance uniformity is considerably simpler for InGaAs than for InP-based integrated circuits. Note also that InGaAs JFETs have smaller values of ξ' than InP JFETs with the same V_p (assuming no tunneling). This is due to the higher V_{DSAT} and smaller g_m' for the InP devices.

These trends are also apparent in Fig.8, which shows ξ' versus pinch-off voltage for InGaAs and InP JFETs assuming the maximum acceptable channel dopings as defined above. The difference in ξ' for these two types of JFETs increases as V_p decreases. Simulation results indicate that InGaAs JFETs have a 40% smaller ξ' than InP JFETs at $V_p = -2V$, with the difference increasing to 75% at $V_p = -5V$.

The experimental data for ξ' listed in Table II are also shown in the plot (solid circles for InGaAs and open circles for InP). Due to the existence of parasitic resistance, the experimental data for the non-self-aligned InP devices are higher than the calculated values. However, the excellent agreement for the experimental InGaAs JFETs with the simulated results, as well as the qualitative agreement for the InP devices, suggests that our model accurately predicts a higher power efficiency for InGaAs transistors. By this criterion, we conclude that the InGaAs JFETs are more

appropriate than the InP JFETs for large-scale monolithic integration, where the power efficiency of each device needs to be maximized.

Returning to Fig. 7, we note that this figure clearly indicates the interrelationship between several FET parameters including channel doping, channel thickness, and pinchoff voltage. For this reason, this plot is useful for predicting the performance of a FET given the various materials parameters. In effect, this plot can be used as a means for designing devices and circuits consisting of either InGaAs or InP FETs. In Paper II we will include the effects of noise in our calculations, and hence obtain further relationships between channel doping and gate *width*. In this manner, complete design criteria specifying all of the various FET parameters can be obtained to predict performance.

The voltage gain of a common source amplifier with a drain load resistance R_L is $A_V \simeq g_m'(R_L//r_o)$, (assuming $A_V >> 1$). Using an active load gain stage such as that shown in the inset in Fig.9a, we obtain $R_L = r_o$. Combining, Eqs.(5) and (10), we obtain:

$$A_V \simeq g_m' r_o/2 \simeq \cosh[\pi(L-L_1)/2a]/2 \qquad (15)$$

Thus, A_V is exponentially dependent on channel thickness, i.e., the thinner the channel, the higher the voltage gain. However, the channel thickness is also related to the pinch-off voltage of the device. Figure 9 shows the voltage gain versus channel doping for InGaAs and InP JFETs at a bias point of $V_{DS} = V_{DSAT} + 1.2$ V and $V_{GS} = 0$, with pinch-off voltage as a parameter. Because of higher g_m' and r_o in InGaAs than in InP JFETs as discussed previously, the InGaAs JFETs show a significantly higher A_V than the InP

JFETs with the same channel doping, when the former devices are not operated in the tunneling regime. However, due to the high breakdown electric field of InP, these latter JFETs can also potentially achieve a high A_V by increasing channel doping. Overall, for the acceptable maximum channel dopings, both devices show the same A_V of ~18. Our calculations are in reasonable agreement with the few examples of A_V reported for InGaAs amplifiers (see, for example, Ref. 33).

The device performance for optimized InGaAs and InP JFETs with L = 1 μm is summarized in Table III. The InP JFET has higher maximum g_m', but also a larger C_{GS} and ξ' than the InGaAs JFET, as described. Here, channel widths of these two devices are assumed to be 150 μm. The optimization of gate width and other parameters needed to achieve the highest performance from optical receivers will be discussed in detail in Paper II.

IV. Conclusion

The optimization model, which considers the effects of band-to-band tunneling and channel resistance for InGaAs and InP JFETs, has been employed as a means for designing high performance InGaAs and InP JFETs for OEIC applications. We have found that a small effective electron mass and narrow band gap make InGaAs more susceptible to tunneling, which limits the maximum allowable channel doping to 7.0×10^{16} cm^{-3}, whereas the channel doping of InP JFETs can approach 5.0×10^{17} cm^{-3}. Such maximum channel dopings can, in principle, result in a transconductance of 220 mS/mm for InGaAs, and 340 mS/mm for InP JFETs. However, both calculations and experimental observations indicate that InGaAs JFETs show a significantly improved power efficiency than obtained for similar InP JFETs. In

addition, the device performance parameters are not as strongly dependent on structure (e.g. channel doping and thickness) for InGaAs as compared with InP-based transistors. Therefore, we conclude that InGaAs JFETs appear to be more suitable for very high density circuit applications than are InP JFETs. However, in view of their similar amplifier gain and cutoff frequencies, in most respects these materials should produce similar results provided that other "extrinsic" parameters (such as source contact resistance) can be made comparable. In the following paper (Paper II), we will discuss the effect that these performance parameters have on the design and characteristics of OEIC receivers. These archetype circuits are presently of considerable interest in photonic systems applications.

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Table I

Summary of Material Parameters

Parameter	Symbol	$In_{0.53}Ga_{0.47}As$	InP
Energy gap at 300 K	E_g(eV)	0.75	1.35
Electron effective mass ratio[a]	m_c^*/m_o	0.041	0.08
Hole effective mass ratio[a]	m_v^*/m_o	0.50	0.56
Peak electron drift velocity[b,c]	v_p(cm/s)	2.7×10^7	2.5×10^7
Electron mobility[d]	μ(cm^2/V-s)	10,000	3,000
Dielectric constant	ϵ_s/ϵ_o	12.0	12.3
Intrinsic carrier concentration at 300K	n_i(cm^{-3})	6.9×10^{11}	1.1×10^7

[a] *GaInAsP Alloy Semiconductors*, T.P. Pearsall Ed. New York: Wiley, 1982

[b] See reference 9

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Table II(a)

Experimental Data for $In_{0.53}Ga_{0.47}As$ JFETs (at $V_{GS} = 0$)

Device	1	2	3	4	5
Parameter:					
$N_D(cm^{-3})$	$1.5x10^{16}$	$2x10^{16}$	$7x10^{16}$	$-9x10^{16}$	$1x10^{17}$
a(A)	~7000	4000	3000	~2800	3000
L(μm)	2	1	1.5	0.5	1
V_p(V)	--7	-2	-1.8	--2.7	-4.0
I_{DS}(mA/mm)	140	96	240	450	440
V_{DS}(V)	5.0	1.5	1.5	1.5	1.5
g_m'(mS/mm)	32	68	210	245	170
C_{GS}(pF/mm)	8.3	~2	--	0.54	2.5
ξ'(W/S)	22	2.1	1.7	2.7	3.9
Ref.	23	18	9	24	25

Table II(b)

Experimental Data for InP JFETs (at V_{GS} = 0)

Device	1	2	3	4	5
$N_D(cm^{-3})$	$3x10^{16}$	$\sim 6x10^{16}$	$\sim 6x10^{16}$	$\sim 1.5x10^{17}$	$1.5x10^{17}$
a(A)	7700	~2500	~2000	~3000	~2000
L(μm)	1	5	2	2	1.5
Vp(V)	-13	-2.8	-2.4	--13	-3.2
I_{DS}(mA/mm)	260	55	60	680	140
V_{DS}(V)	8.0	5.0	3.5	5.0	3.5
g_m'(mS/mm)	>35	~40	50	~90	90
C_{GS}(pF/mm)	<0.7	3.8	1.2	--	1.5
ξ'(W/S)	59	6.9	4.?	38	5.4
Ref.	26	27	28	10	11

Table III

Performance summary of optimized $In_{0.53}Ga_{0.47}As$ and InP JFETs[a]

Parameter	Symbol	$In_{0.53}Ga_{0.47}As$	InP
Channel Carrier Concentration	$N_D(cm^{-3})$	$7x10^{16}$	$5x10^{17}$
Channel thickness	a(A)	2300	950
Channel length	L(μm)	1	1
Channel width	Z(μm)	150	150
Pinch-off voltage	V_p(V)	-2	-2
Drain current	I_{DS}(mA/mm)	300	500
Drain voltage	V_{DS}(V)	1.6	2.0
Transconductance	g_m'(mS/mm)	220	340
Power dissipated per transconductance	ξ'(W/S)	2.1	2.9
Gate-source capacitance	C_{GS}(pF/mm)	0.84	1.5
Output resistance	r_o(Ω-mm)	162	104
Voltage gain	A_v	18	18
Cut-off frequency	f_T(GHz)	40	35

[a]Operating point is assumed at V_{GS} = 0 V and V_{DS} = V_{DSAT}+1.2V as described in text.

Figure Captions

Fig. 1a: Cross-section of a self-aligned JFET and equivalent circuit elements.

Fig. 1b: A confined-area-channel JFET (CAC-JFET) structure with high source and drain dopings to reduce contact resistances.

Fig. 2: Comparison of simulation results (solid lines) and experimental data (dots) obtained from (a) Cheng, et al. [18] for an InGaAs JFET, and from (b) Boos' et al. [10] for an InP JFET. The saturation voltage, V_{DSAT}, is indicated by the dashed lines.

Fig. 3: The bias voltage corresponding to a tunneling current density of 1 mA/cm^2 and avalanche breakdown voltage as functions of impurity concentration for InGaAs and InP assuming abrupt p^+-n junctions.

Fig. 4: Degradation of transconductance due to the effect of tunneling for 1 μm long gate InGaAs JFET with $N_D = 1.5 \times 10^{17}$ cm^{-3}. The solid lines indicate the transconductance for which the effects of tunneling are neglected, whereas the dashed lines show the transconductance in the presence of tunneling.

Fig. 5: Transconductance for 1 μm long gate InGaAs, InP and GaAs JFETs as a function of channel doping. Solid and open circles correspond to experimental data listed in Table II obtained for InGaAs and InP JFETs, respectively.

Fig. 6: Output resistance as a function of channel doping for 1 μm long gate (a) InGaAs and (b) InP JFETs with pinch-off voltage as a parameter.

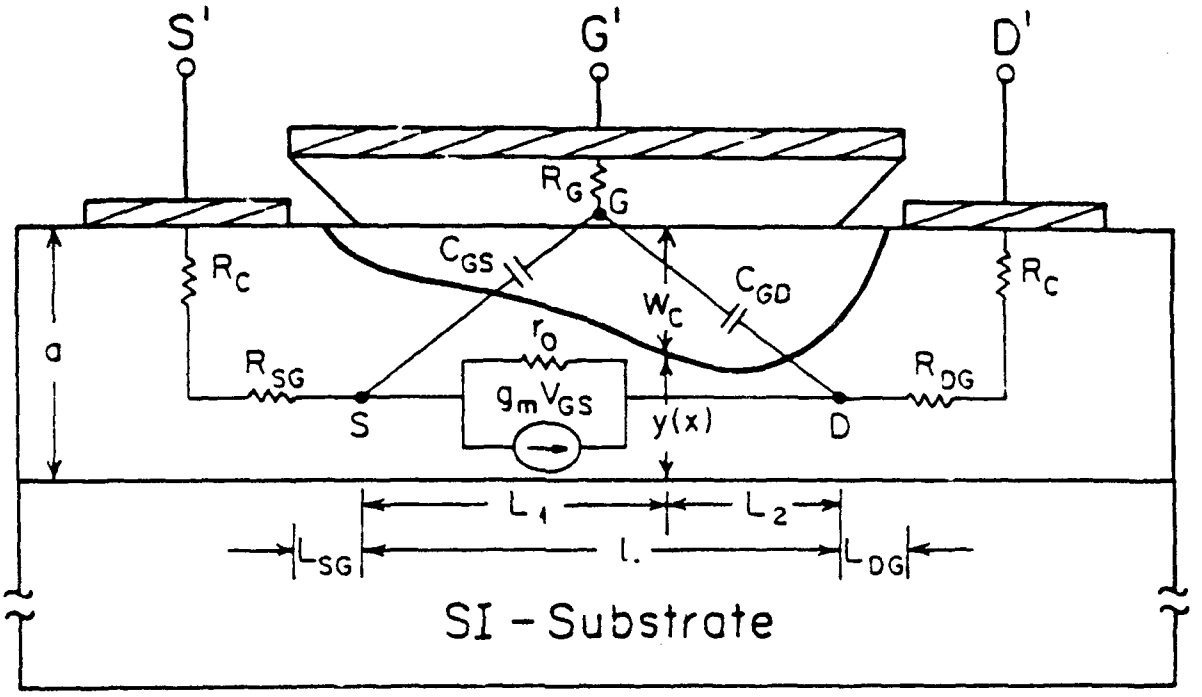
Fig. 7: Power dissipated per transconductance (ξ') for 1 μm long gate

(a) InGaAs and (b) InP JFETs as a function of channel doping, with channel thickness (a) and pinch-off voltage (V_p) as parameters.

Fig. 8: Power dissipated per transconductance (ξ') of optimized devices as a function of pinch-off voltage. Solid and dashed curves show the simulation results, and solid and open circles indicate the experimental data for InGaAs and InP JFETs, respectively.

Fig. 9: Voltage gain of the common source amplifiers circuit shown in the inset as a function of channel doping for (a) InGaAs and (b) InP JFETs.

(a)


S'
G'
D'
R_G
G
C_{GS}
C_{GD}
R_C
R_C
W_C
a
r_o
R_{SG}
$g_m V_{GS}$
R_{DG}
S
y(x)
D
L_1
L_2
L_{SG}
l.
L_{DG}
SI - Substrate

(b)

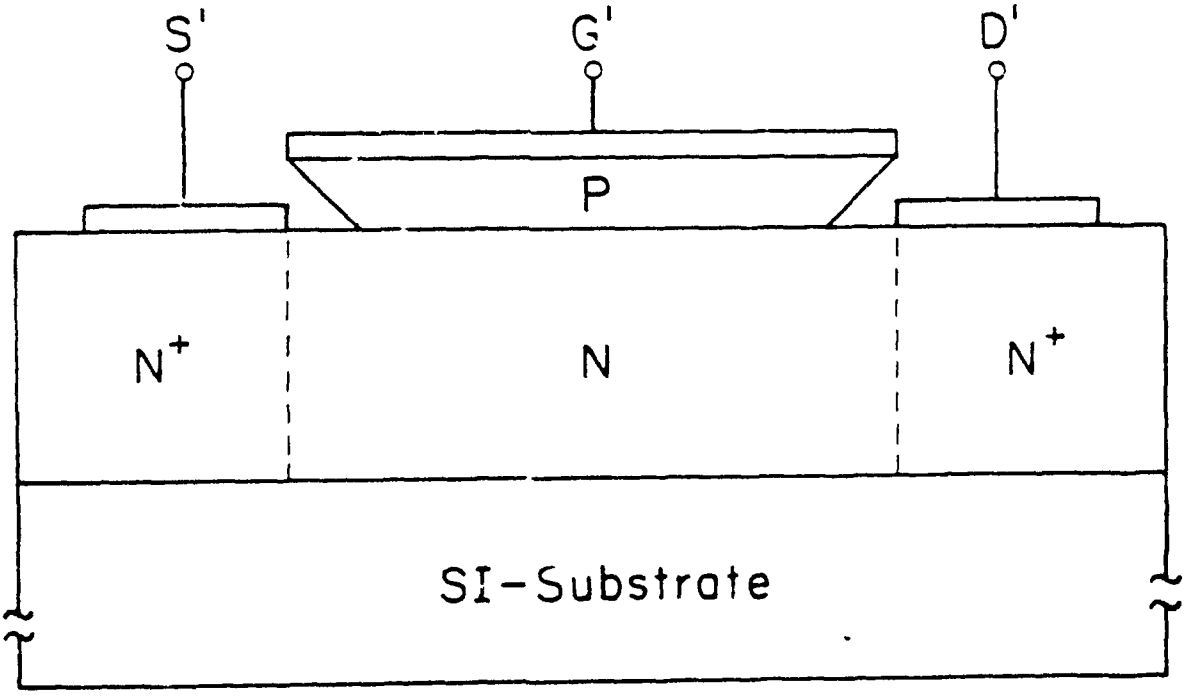

S'
G'
D'
P
N^+
N
N^+
SI-Substrate

Fig. 1

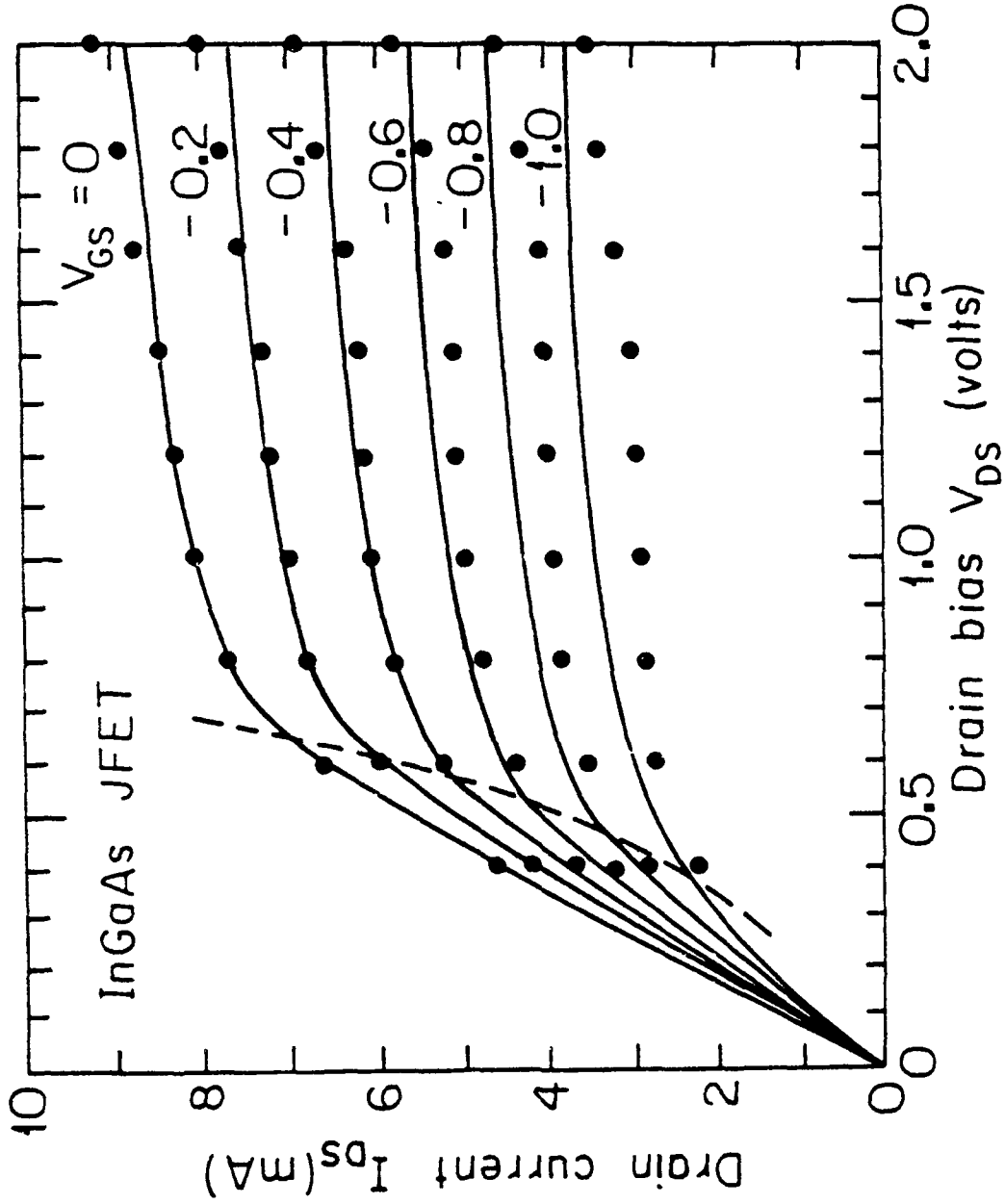

InGaAs JFET
V_{GS} = 0
-0.2
-0.4
-0.6
-0.8
-1.0
Drain current I_{ds}(mA)
Drain bias V_{DS} (volts)
0
2
4
6
8
10
0
0.5
1.0
1.5
2.0

Fig 2(a)

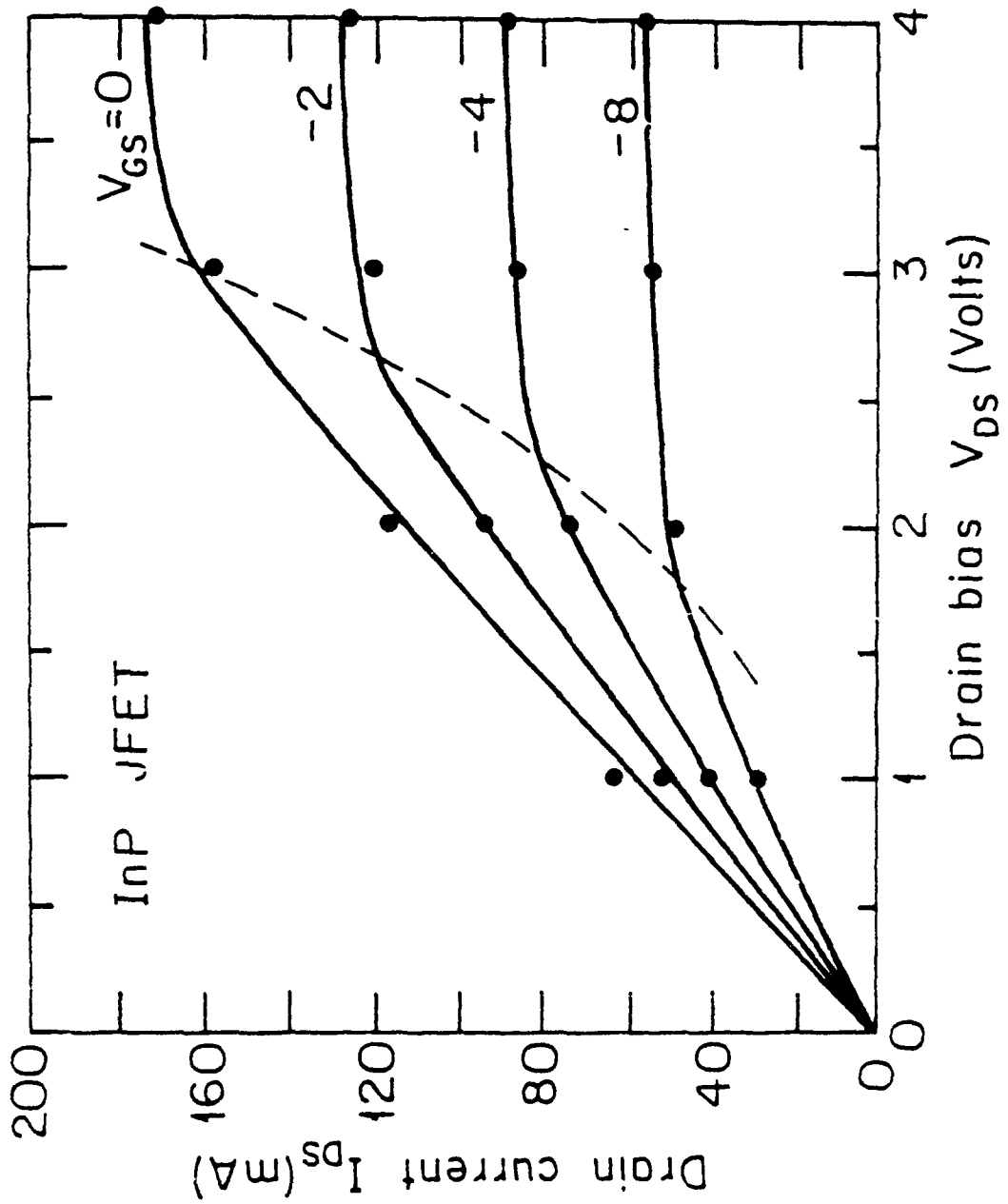

InP JFET
V_{GS}=0
-2
-4
-8
Drain current I_{DS}(mA)
Drain bias V_{DS} (Volts)
0
40
80
120
160
200
0
1
2
3
4

Fig 2(b).

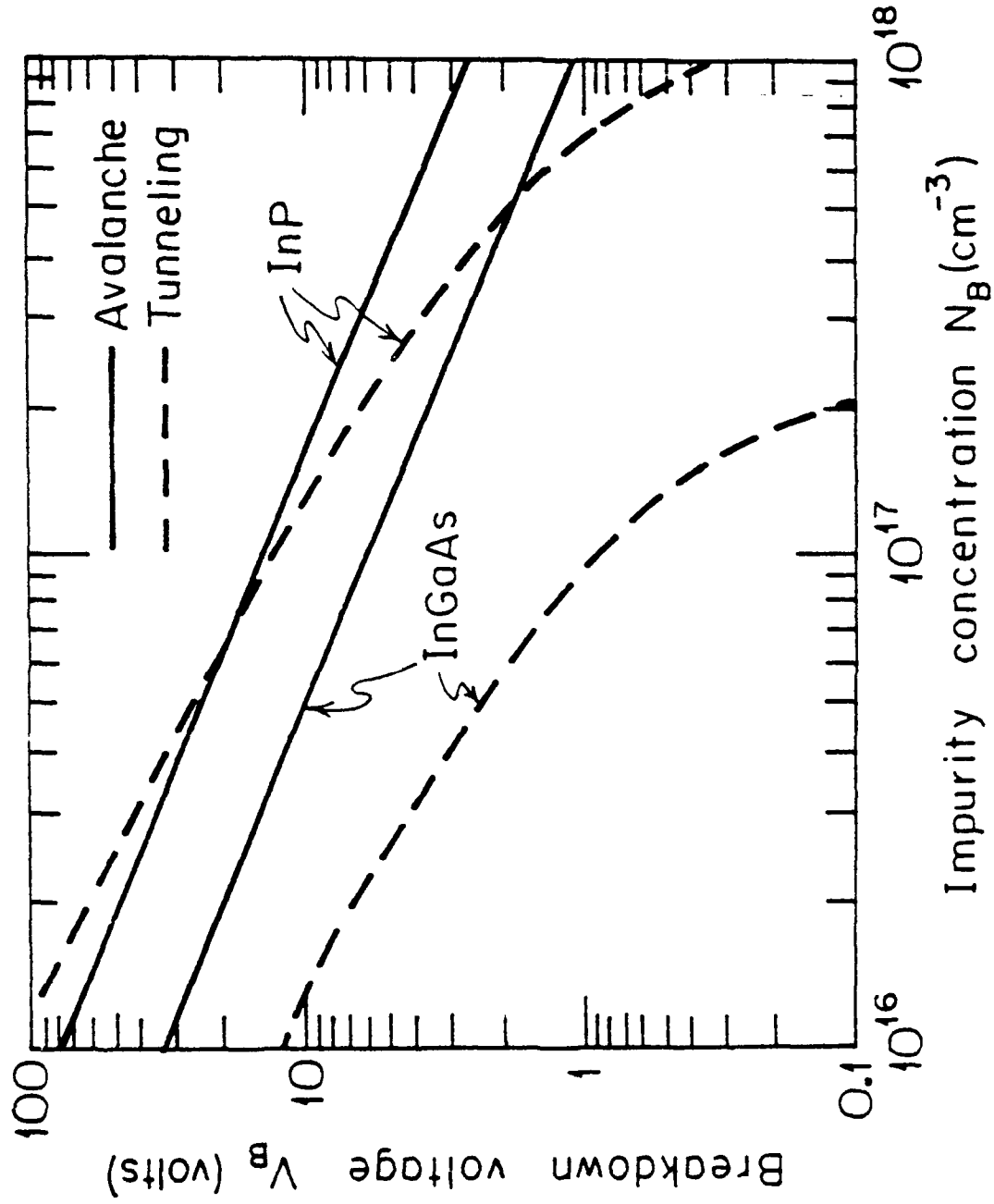

Avalanche
Tunneling
InP
InGaAs
100
10
1
0.1
10^{16}
10^{17}
10^{18}
Breakdown voltage V_B (volts)
Impurity concentration $N_B(cm^{-3})$

Fig. 3

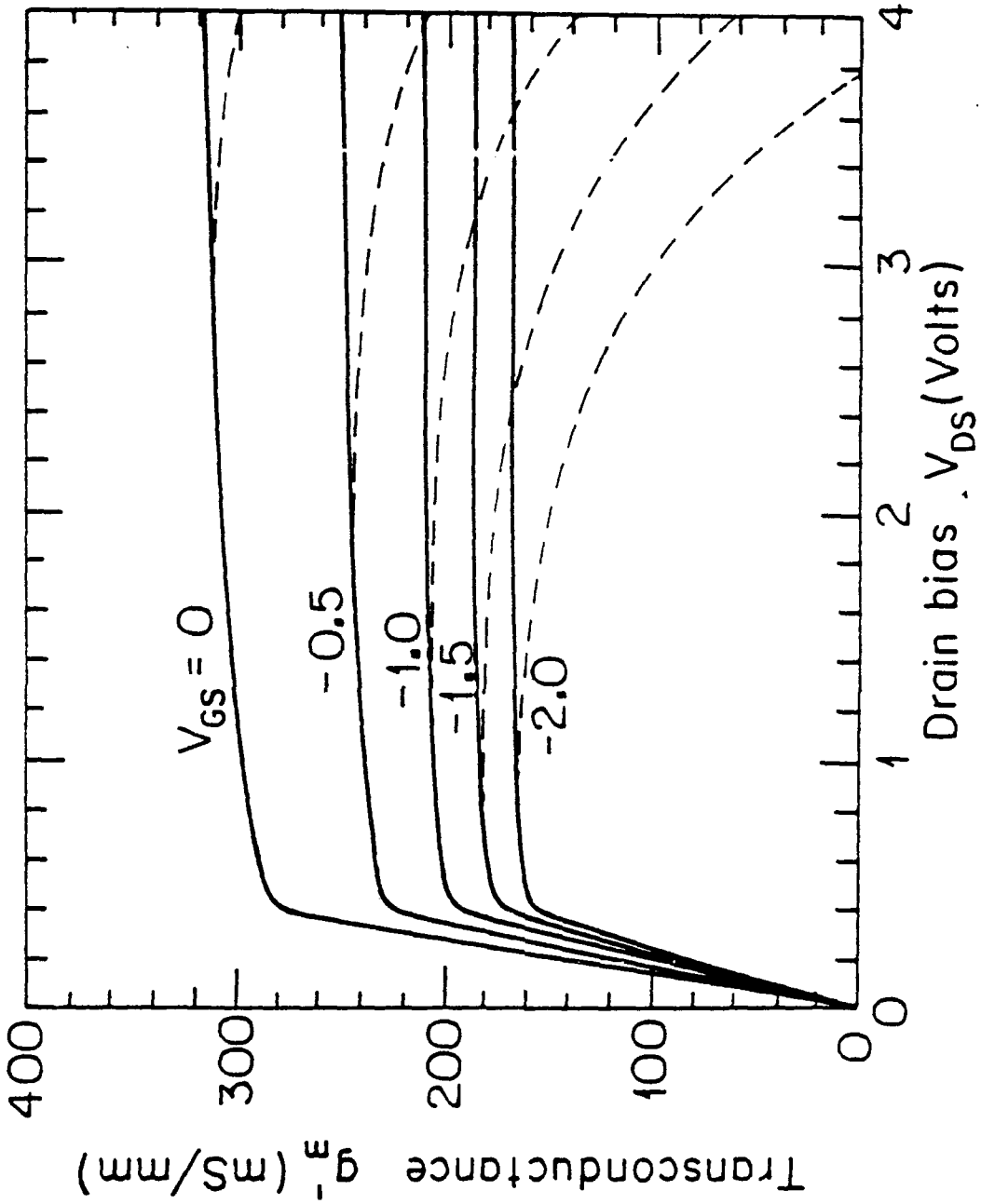

Transconductance g_m (mS/mm)
400
300
200
100
0
0
1
2
3
4
Drain bias, V_{DS} (Volts)
V_{GS} = 0
-0.5
-1.0
-1.5
-2.0

Fig. 4

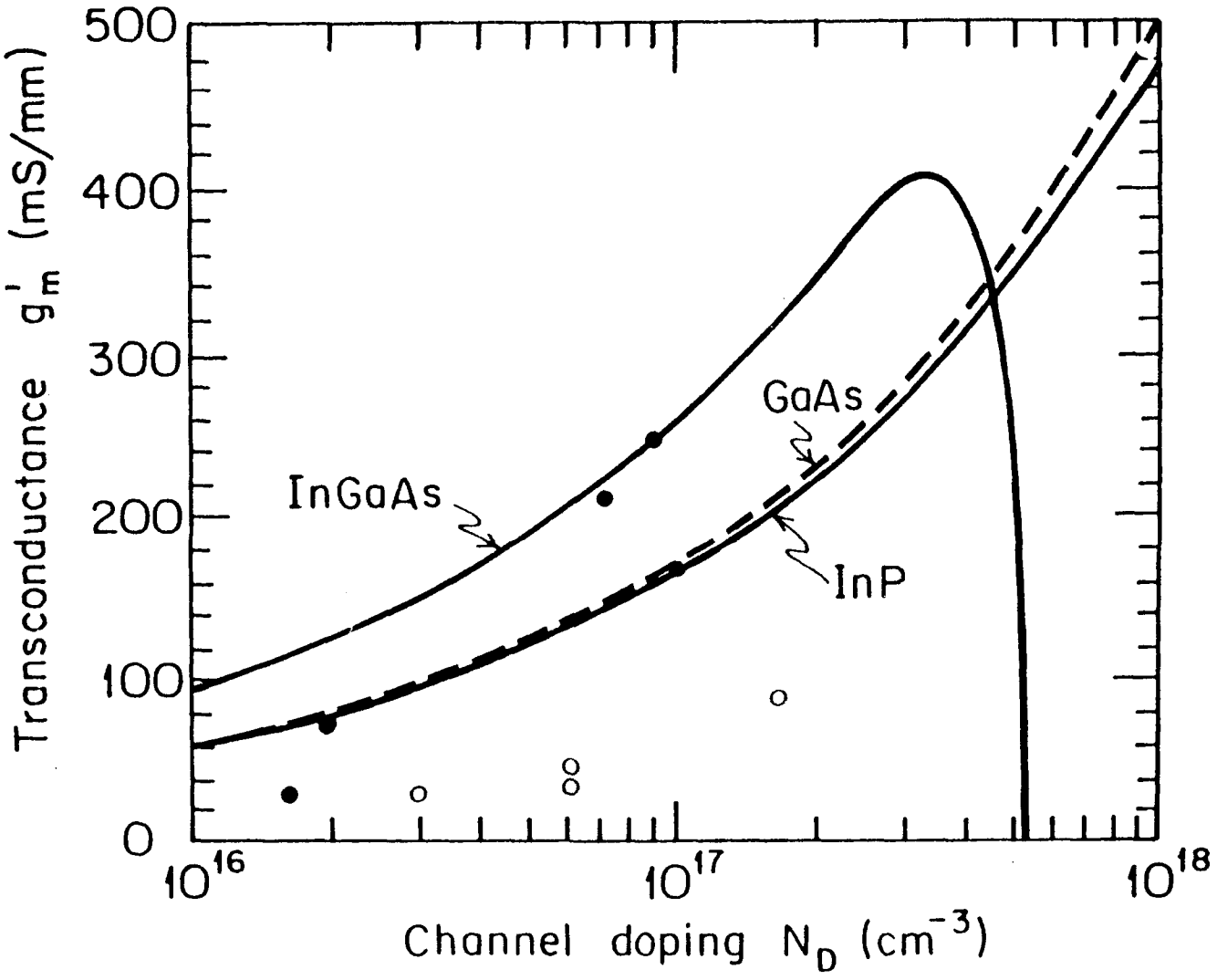

500
400
300
200
100
0
Transconductance g_m' (mS/mm)
InGaAs
GaAs
InP
10^{16}
10^{17}
10^{18}
Channel doping N_D (cm^{-3})

Fig 5

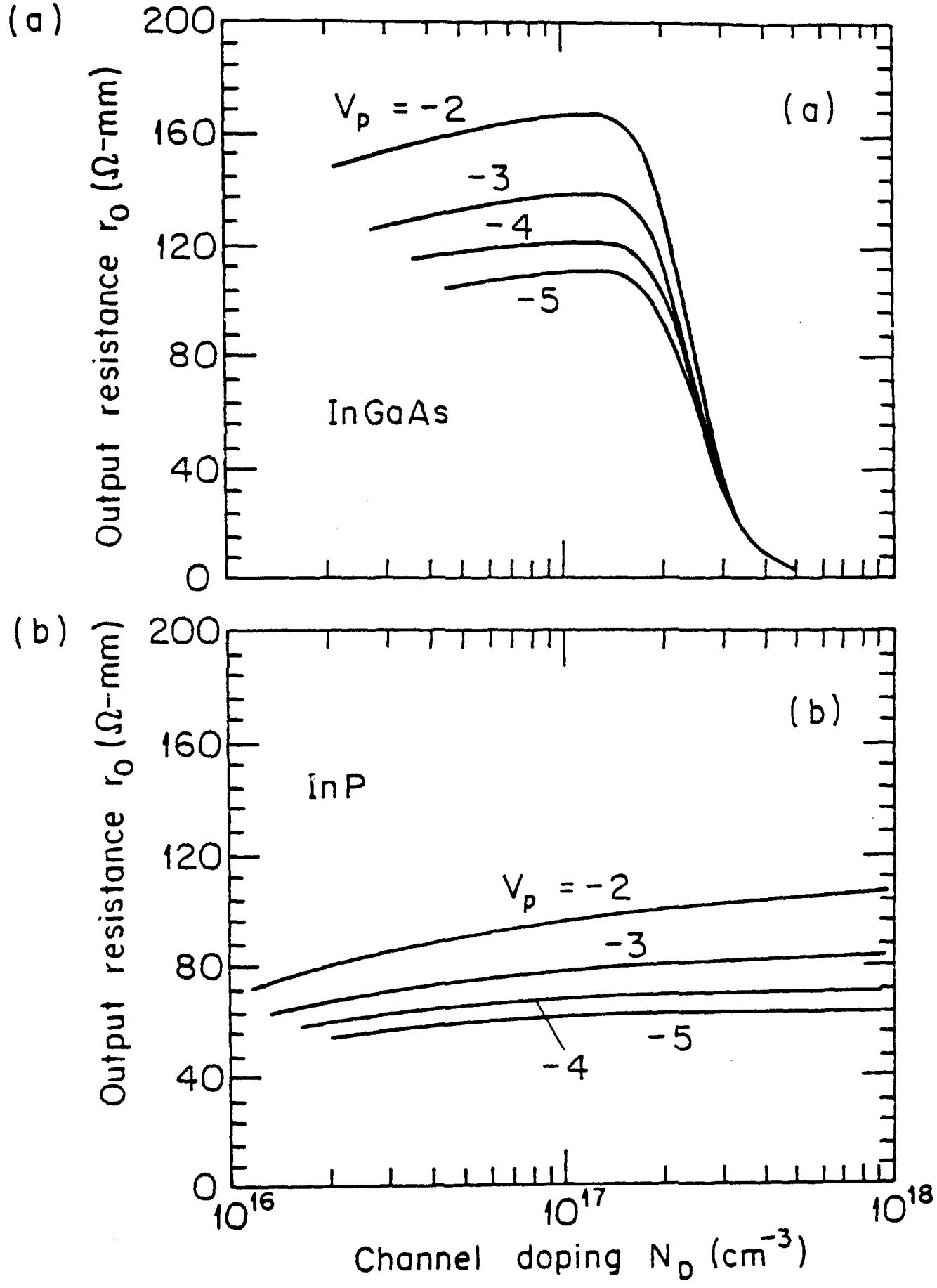

(a)
200
160
120
80
40
0
Output resistance r_o (Ω-mm)
V_p = -2
-3
-4
-5
(a)
InGaAs
(b)
200
160
120
80
40
0
Output resistance r_o (Ω-mm)
(b)
InP
V_p = -2
-3
-4
-5
10^{16}
10^{17}
10^{18}
Channel doping N_D (cm^{-3})

Fig. 6

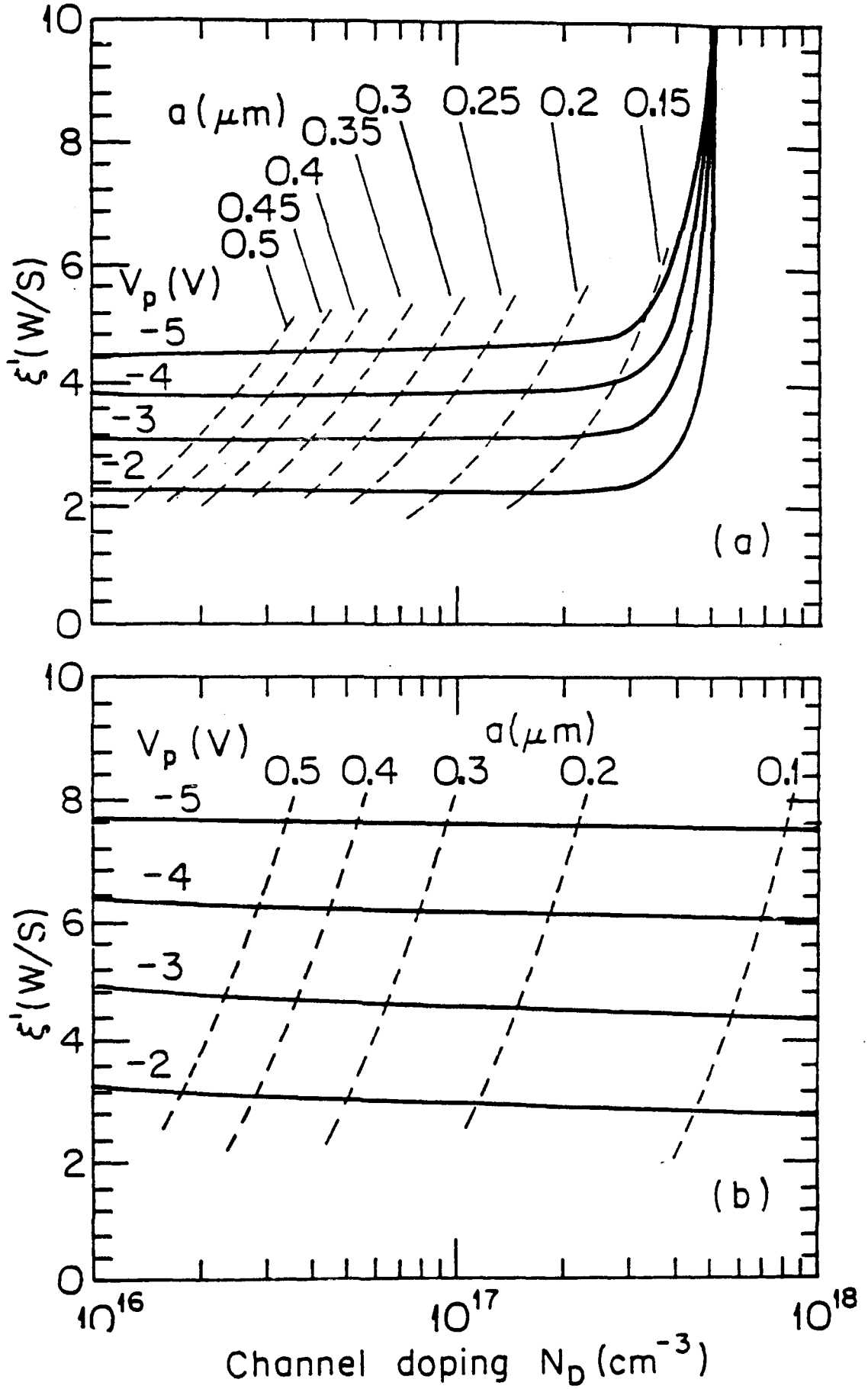

10
8
6
4
2
0
a(μm)
0.3
0.25
0.2
0.15
0.35
0.4
0.45
0.5
Vp(V)
-5
-4
-3
-2
ξ'(W/S)
(a)
Vp(V)
a(μm)
0.5
0.4
0.3
0.2
0.1
(b)
10^16
10^17
10^18
Channel doping ND (cm^-3)

Fig. 7

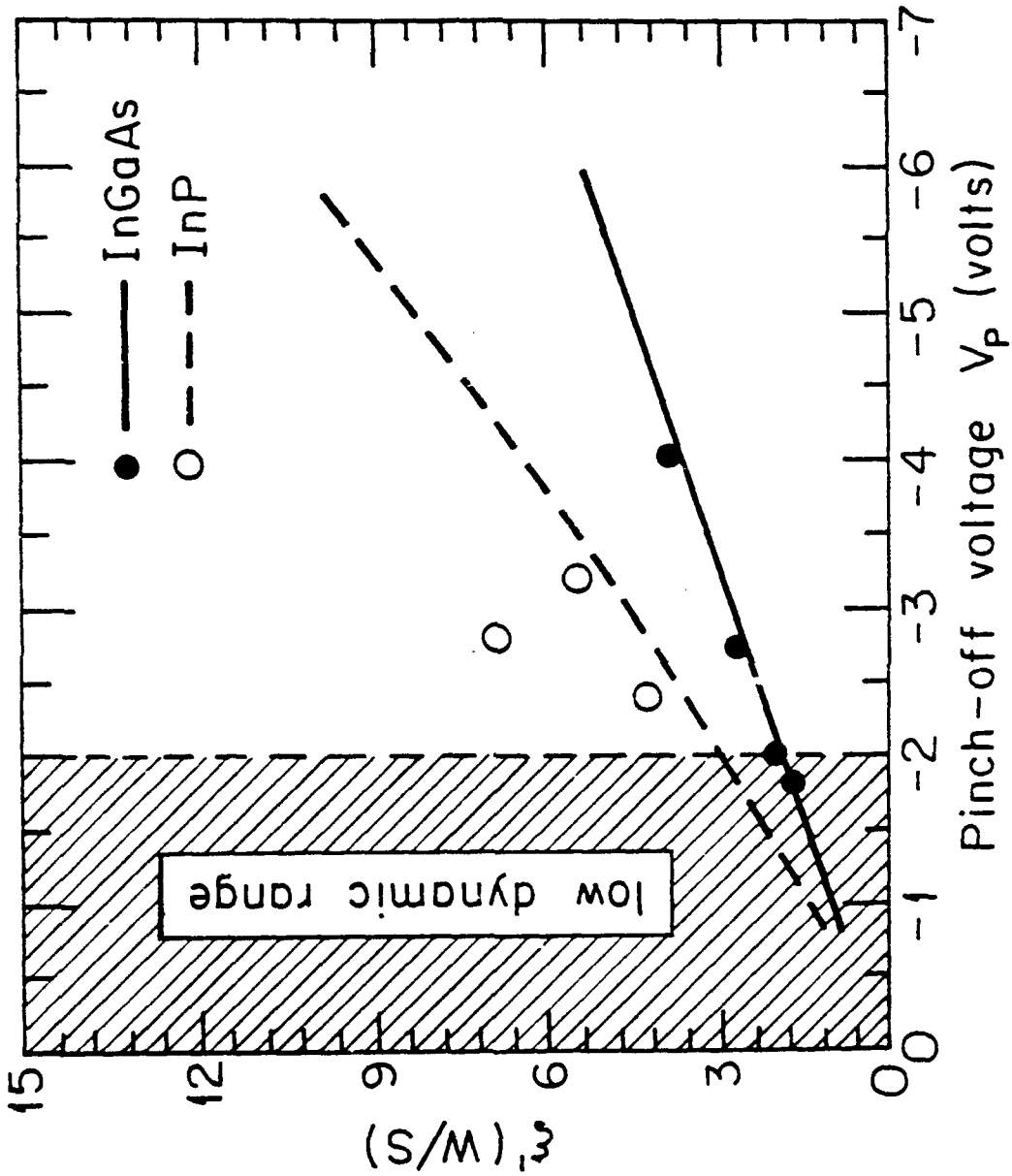

InGaAs
InP
low dynamic range
ε'(W/S)
Pinch-off voltage V_p (volts)
15
12
9
6
3
0
0
-1
-2
-3
-4
-5
-6
-7

Fig. 8

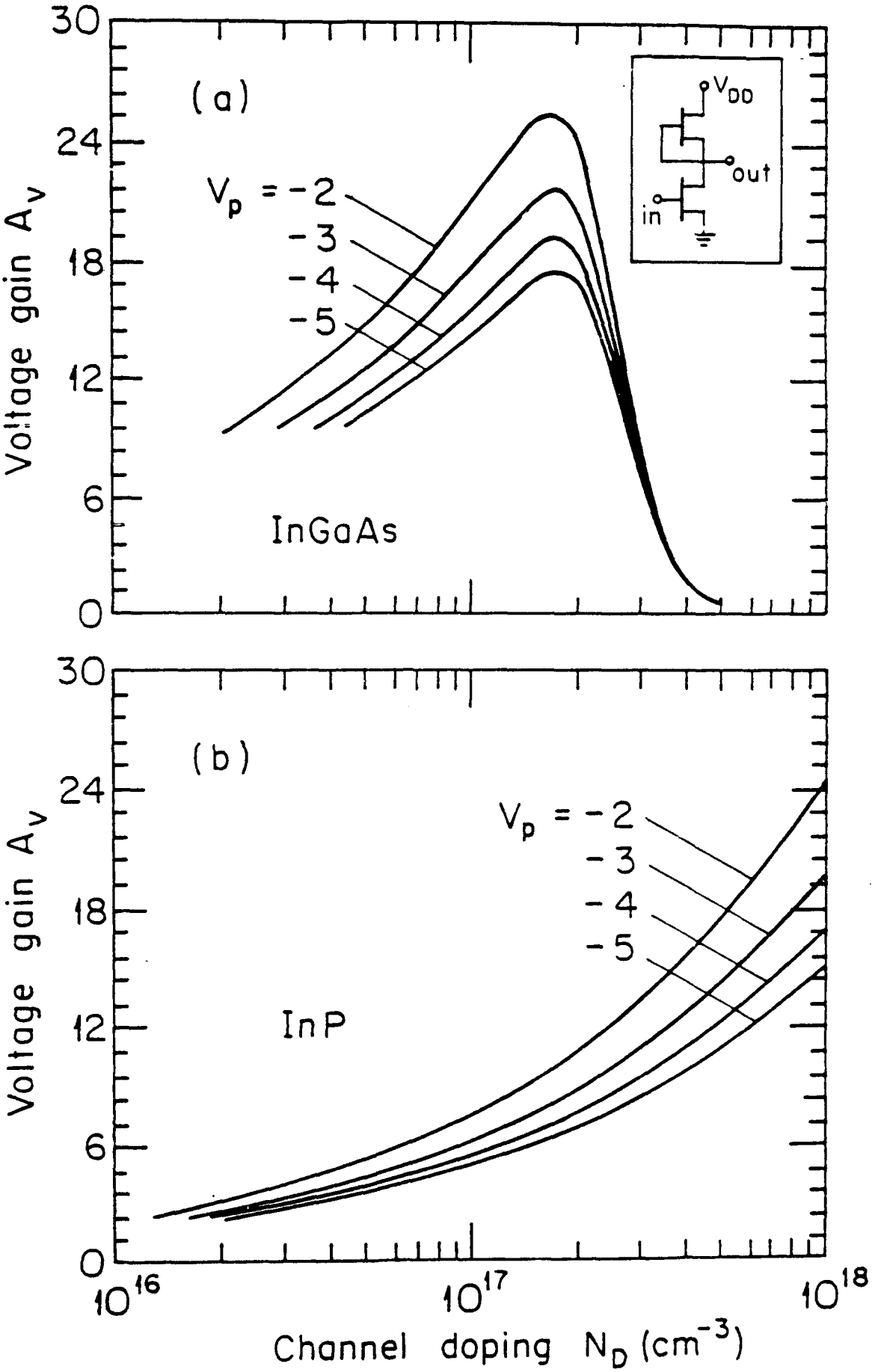

(a)
V_p = -2
-3
-4
-5
InGaAs
Voltage gain A_v
30
24
18
12
6
0
V_{DD}
out
in
(b)
V_p = -2
-3
-4
-5
InP
Voltage gain A_v
10^{16}
10^{17}
10^{18}
Channel doping N_D (cm^{-3})

Fig. 9

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